ENCLUSTRA
FPGA SOLUTIONS

Catalogue Autumn 2021

SoC and FPGA Modules

Andromeda XZU90. Unprecedented performance, with Zynq® UltraScale+™

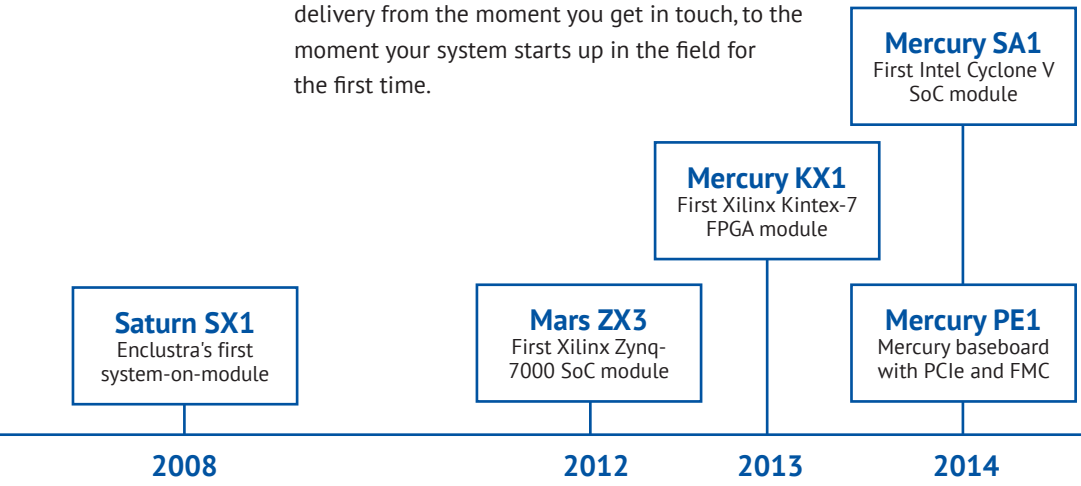
Everything FPGA.

Everything FPGA.

At Enclustra, everything is FPGA.

Our products are used by more than 1600 customers in over 70 countries, and our customer base is growing quickly. We don't develop hardware and IP products only – **we do customer design projects too;** every stage of development, from conception through to bring-up at the customer site. We have more than 17 years of FPGA system design under our belt; break it down a little further and our team of engineers has far in excess of 300 person years of FPGA experience.

Our expertise enables us to create the best experience for our customers. We pride ourselves on the quickest, highest possible quality of service and delivery from the moment you get in touch, to the moment your system starts up in the field for the first time.

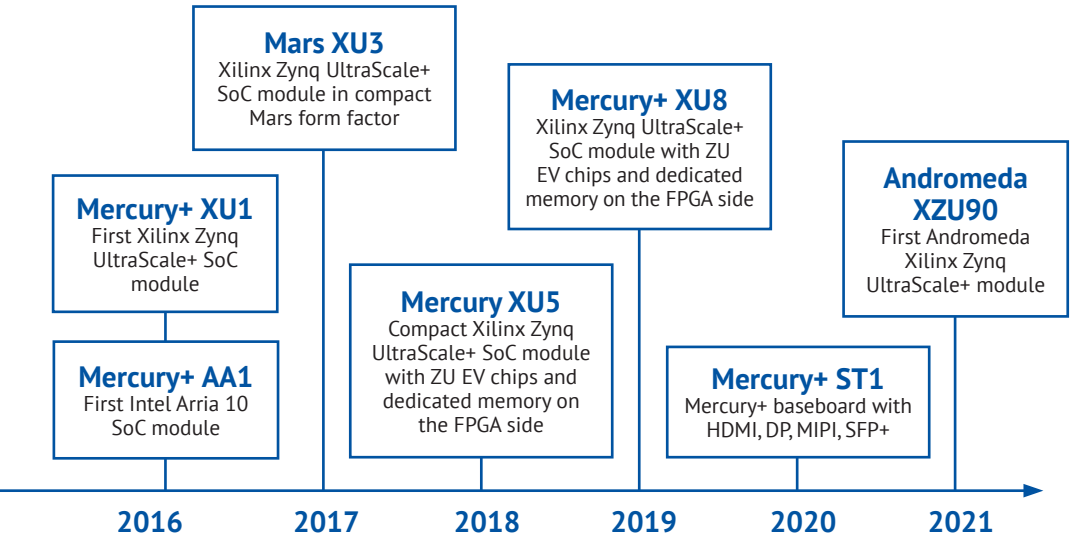


Our off-the-shelf SoC & FPGA modules are developed with the aim of simplifying the overall design of your FPGA-based system, thus significantly reducing the time and cost to market.

As with our product range and our customer base, our list of completed projects is growing – to keep up with developments, and not miss any of our upcoming innovations, subscribe to our newsletter at **www.enclustra.com/subscribe**

This catalogue presents our current product and services; if anything piques your interest, don't hesitate to get in touch.

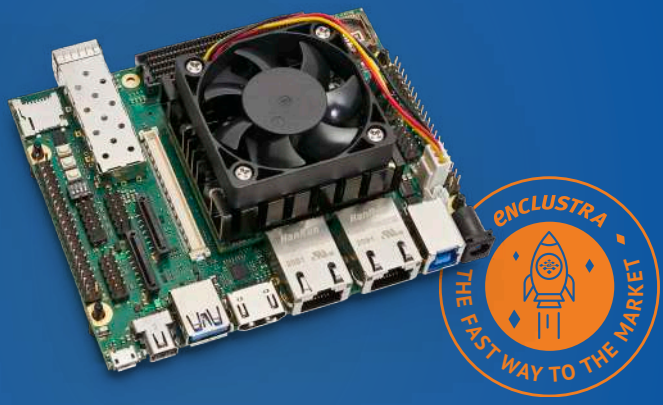
Thanks! The Enclustra Team.



DESIGN-IN KIT

AI/Machine Learning Examples Included

The Enclustra Design-in Kits help shorten time-to-market for any Xilinx Zynq UltraScale+ MPSoC based application. Be it image processing, machine vision, test & measurement, communication or medical: With an Enclustra System-on-Module, the development time can be halved.



What's Inside the Box

- Enclustra Xilinx Zynq UltraScale+ MPSoC module (Mercury XU5 or Mars XU3)
- Base board (Mercury+ ST1 or Mars ST3)
- USB camera
- Heatsink
- Fan
- Power supply
- USB cable
- MiniDP to DP cable
- Micro SD card
- Example applications:
  - AI face detection
  - Image classification
- Quick start guide
- User Manual

Available Resources

- Documentation
- Design support
- Design-in kit user guide
- User manuals
- Reference design
- PetaLinux board support package (BSP)
- Buildroot-based Linux BSP
- Module pin connection guidelines
- Master pinout
- Footprints
- 3D model
- IO net length
- User schematics
- Altium design files (base board)
- Application notes

» Contents

Enclustra Products
Delivered fast; made to last

Our modules all come with a minimum expected **lifetime of 10+ years;** seeing as we also design our products with forward-looking availability and performance in mind, this means you can depend on our products to deliver over the long term.

Our modules belonging to the same product family are largely pin-compatible, meaning you can also plan a clear upgrade path. A full selection guide and roadmap can be found after the individual module info pages.

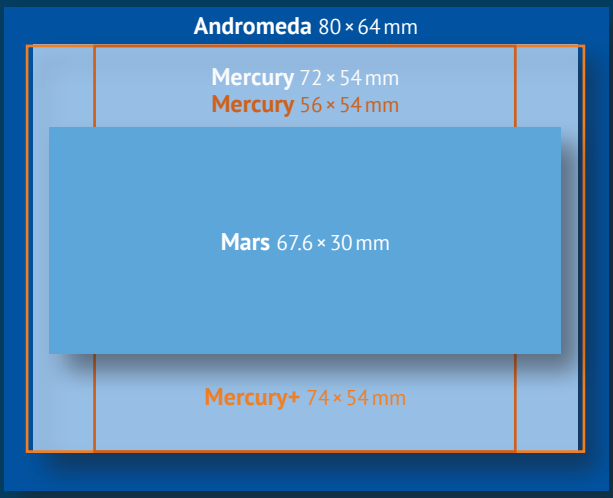
» Chip-based Product Table

FPGA Device Family	FPGA Device	Enclustra Product Series	Pages
XILINX			
Zynq® UltraScale+™	ZU2CG	Mercury XU5, Mercury+ XU6, Mars XU3	11, 12, 23
Zynq® UltraScale+™	ZU2EG	Mercury XU5, Mercury+ XU6, Mars XU3	11, 12, 23
Zynq® UltraScale+™	ZU3EG	Mercury XU5, Mercury+ XU6, Mars XU3	11, 12, 23
Zynq® UltraScale+™	ZU4CG	Mercury XU5, Mercury+ XU6, Mercury+ XU8, Mercury+ XU9	11, 12, 14, 15
Zynq® UltraScale+™	ZU4EV	Mercury XU5, Mercury+ XU6	11, 12,
Zynq® UltraScale+™	ZU5EV	Mercury XU5, Mercury+ XU6, Mercury+ XU8, Mercury+ XU9	11, 12, 14, 15
Zynq® UltraScale+™	ZU6CG	Mercury+ XU1	10
Zynq® UltraScale+™	ZU6EG	Mercury+ XU1, Mercury+ XU7	10, 13
Zynq® UltraScale+™	ZU7EG	Andromeda XZU65	25
Zynq® UltraScale+™	ZU7EV	Mercury+ XU8, Mercury+ XU9, Andromeda XZU65	14, 15, 25
Zynq® UltraScale+™	ZU9EG	Mercury+ XU1, Mercury+ XU7	10, 13
Zynq® UltraScale+™	ZU11EG	Andromeda XZU65	25
Zynq® UltraScale+™	ZU15EG	Mercury+ XU1, Mercury+ XU7	10, 13
Zynq® UltraScale+™	ZU17EG	Andromeda XZU90	24
Zynq® UltraScale+™	ZU19EG	Andromeda XZU90	24
Zynq®-7000	7Z010	Mars ZX2	21
Zynq®-7000	7Z015	Mercury ZX5	17
Zynq®-7000	7Z020	Mars ZX2, Mars ZX3	21, 22
Zynq®-7000	7Z030	Mercury ZX1, Mercury ZX5	16, 17
Zynq®-7000	7Z035	Mercury ZX1	16
Zynq®-7000	7Z045	Mercury ZX1	16
Kintex®-7	7K160T	Mercury+ KX2	19
Kintex®-7	7K410T	Mercury+ KX2	19
Artix®-7	A35T	Mars AX3	20
Artix®-7	A50T	Mars AX3	20
Artix®-7	A100T	Mars AX3	20
intel			
Cyclone® V SX	5CSXFC6	Mercury SA1, Mars MA3	29, 26
Cyclone® V ST	5CSTFD6	Mercury+ SA2	28
Arria® 10 SX	10AS027	Mercury+ AA1	27
Arria® 10 SX	10AS048	Mercury+ AA1	27
MICROCHIP			
PolarFire® SoC	MPFS250TS	Mercury+ MP1	30
PolarFire® SoC	MPFS460TS	Mercury+ MP1	30

» Module Overview

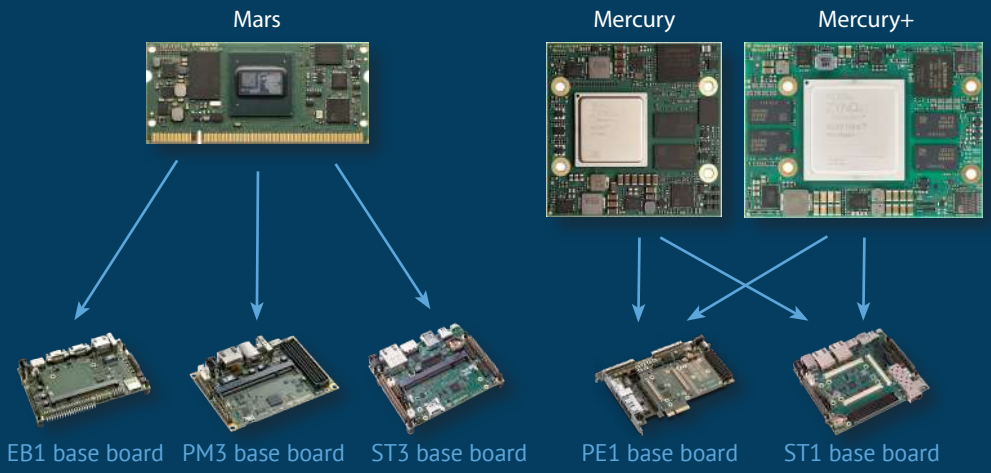
Mars Form Factor 200 Pin SO-DIMM	Mercury Form Factor High Performance	Mercury+ Form Factor High I/O Count & Performance	Andromeda Form Factor Rugged High-End Form Factor & High Bandwidth
Mars XU3 Xilinx Zynq UltraScale+ MPSoC	**Mercury XU5** Xilinx Zynq UltraScale+ MPSoC	**Mercury+ XU8** Xilinx Zynq UltraScale+ MPSoC	**Andromeda XZU90** Zynq UltraScale+ SoC
Mars ZX3 Xilinx Zynq-7000 SoC	**Mercury ZX1** Xilinx Zynq-7000 SoC	**Mercury+ XU1** Xilinx Zynq UltraScale+ MPSoC	**Andromeda XZU65** Zynq UltraScale+ SoC
Mars ZX2 Xilinx Zynq-7000 SoC	**Mercury ZX5** Xilinx Zynq-7000 SoC	**Mercury+ XU7** Xilinx Zynq UltraScale+ MPSoC	
Mars AX3 Xilinx Artix-7		**Mercury+ XU9** Xilinx Zynq UltraScale+ MPSoC	
		Mercury+ KX2 Xilinx Kintex-7	
Mars MA3 Intel Cyclone V SoC	**Mercury SA1** Intel Cyclone V SoC	**Mercury+ AA1** Intel Arria 10 SoC	
		Mercury+ SA2 Intel Cyclone V SoC	
		Mercury+ MP1 Microchip PolarFire SoC	

» Form Factor



1:1 ratio

» Base Board Matching Guide

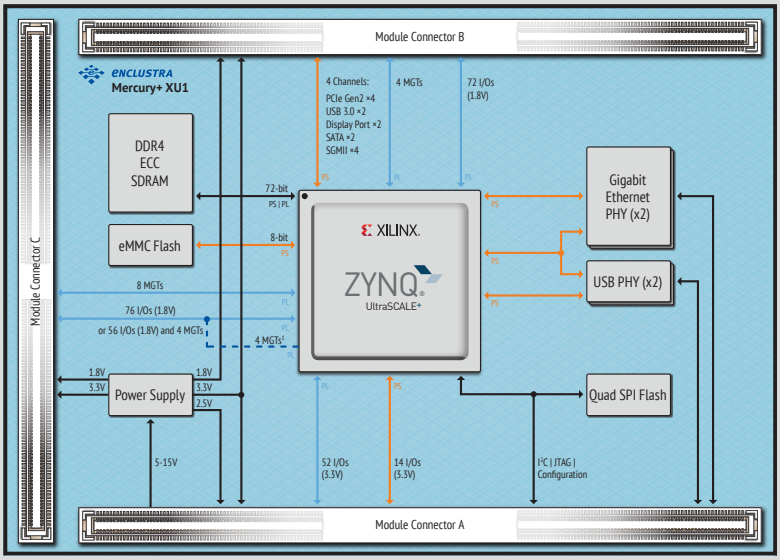


MERCURY+ XU1

Zynq® UltraScale+™ SoC Module

OS support:

- Xilinx® Zynq UltraScale+ MPSoC
- ZU6CG/ZU6EG/ZU9EG/ZU15EG devices
- Dual-/Quad-core ARM® Cortex™-A53
- Dual-core ARM Cortex-R5
- Up to 8 GB DDR4 ECC SDRAM (PS side)
- 64 MB QSPI flash
- 16 GB eMMC flash
- PCIe® Gen2 × 4
- Up to 20 × 6/12.5/15 Gbps MGT
- 2 × Gigabit Ethernet
- 2 × USB 2.0/3.0
- Up to 747,000 system logic cells
- 294 user I/Os
- 5–15 V supply
- 74 × 54 mm



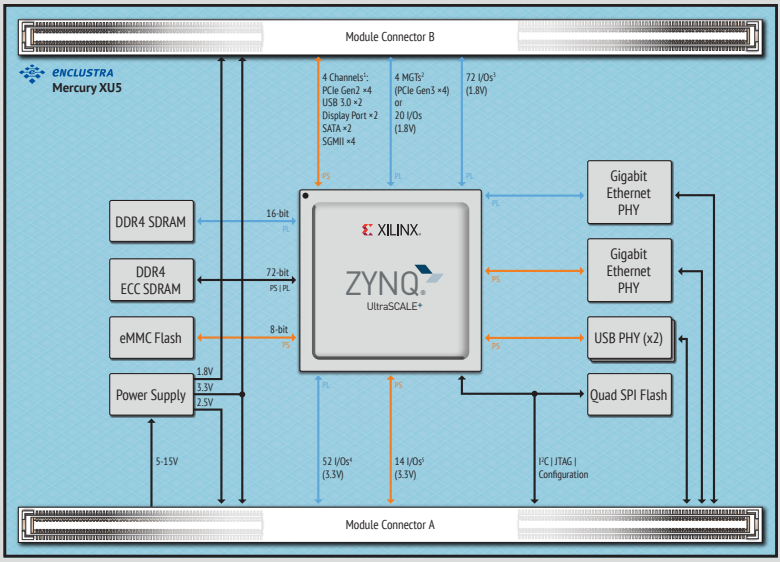
1: G1 assembly variant available starting with revision 3.

MERCURY XU5

Zynq® UltraScale+™ SoC Module

OS support:

- Xilinx® Zynq UltraScale+ MPSoC
- ZU2CG/ZU2EG/ZU3EG/ZU4CG/ZU4EV/ZU5EV devices
- Dual-/Quad-core ARM® Cortex™-A53
- Dual-core ARM Cortex-R5
- H.264 / H.265 Video Codec (EV only)
- Up to 8 GB DDR4 ECC SDRAM (PS side)
- Up to 2 GB DDR4 SDRAM (PL side)
- 16 GB eMMC flash
- 64 MB QSPI flash
- PCIe Gen2 × 4
- PCIe Gen3 × 4 (only devices larger than ZU3)
- Up to 8 × 6/12.5 Gbit/sec MGT
- 2 × Gigabit Ethernet
- 2 × USB 2.0/3.0
- Up to 256,000 system logic cells
- 178 user I/Os
- 5–15 V supply
- 56 × 54 mm



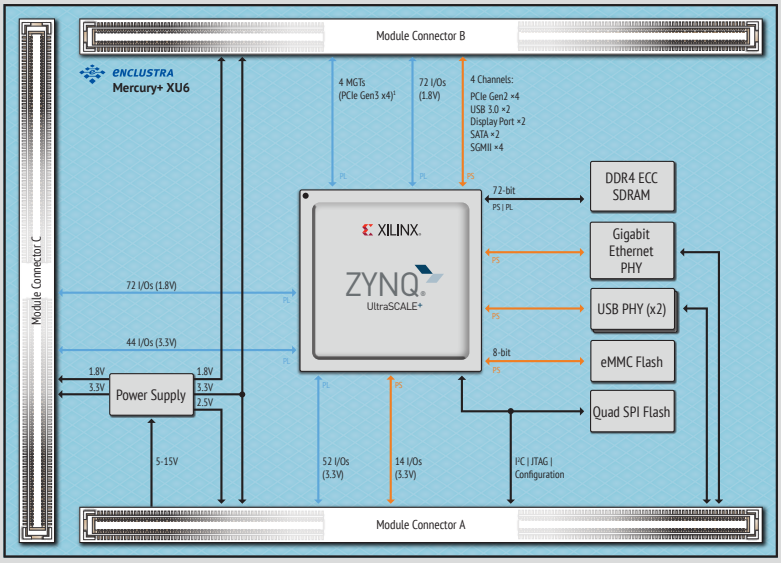
G1 Variants: 1.) 0 Channels, 2.) 4 MGTs only, 3.) 92 I/Os, 4.) 54 I/Os, 5.) 12 I/Os

MERCURY+ XU6

Zynq® UltraScale+™ SoC Module

OS support:

- Xilinx® Zynq UltraScale+ MPSoC
- ZU2CG/ZU2EG/ZU3EG/ZU4CG/ZU4EV/ZU5EV devices
- Dual-/Quad-core ARM® Cortex™-A53
- Dual-core ARM Cortex-R5
- H.264 / H.265 Video Codec (EV only)
- Up to 8 GB DDR4 SDRAM (PS side)
- 16 GB eMMC flash
- 64 MB QSPI flash
- Up to 8 × 6/12.5 Gbps MGT
- PCIe Gen2 × 4
- PCIe® Gen3 × 4 (only devices larger than ZU3)
- Gigabit Ethernet
- 2 × USB 2.0/3.0
- Up to 256,000 system logic cells
- Up to 294 user I/Os
- 5–15 V supply
- 65 × 54 mm



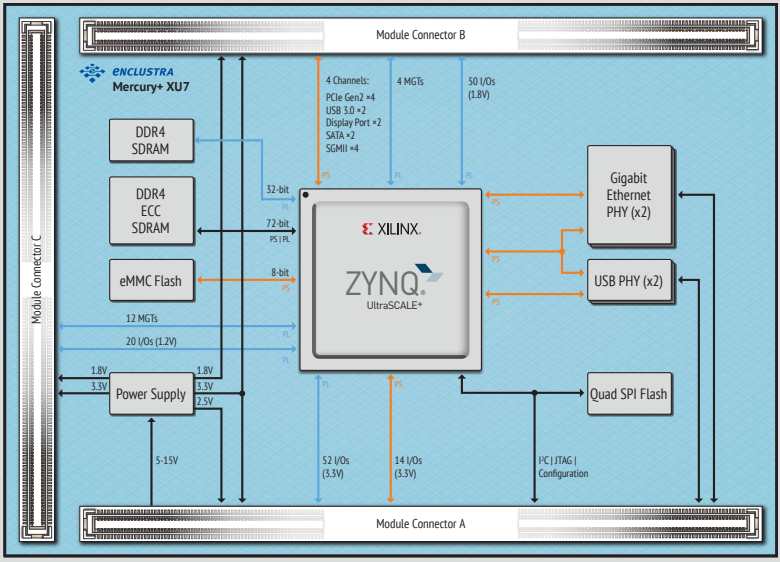
1: MGTs and PCIe support only for FPGA devices larger than ZU3
Early Access – please contact us for availability.

MERCURY+ XU7

Zynq® UltraScale+™ SoC Module

OS support:

- Xilinx® Zynq UltraScale+ MPSoC
- ZU6EG/ZU9EG/ZU15EG devices
- Dual-/Quad-core ARM® Cortex™-A53
- Dual-core ARM Cortex-R5
- Up to 8 GB DDR4 ECC SDRAM (PS side)
- Up to 4 GB DDR4 SDRAM (PL side)
- 16 GB eMMC flash
- 64 MB QSPI flash
- PCIe Gen2 × 4
- 20 × 6/12.5/15 Gbps MGT
- 2 × Gigabit Ethernet
- 2 × USB 2.0/3.0
- Up to 747,000 system logic cells
- 236 user I/Os
- 5–15 V supply
- 74 × 54 mm

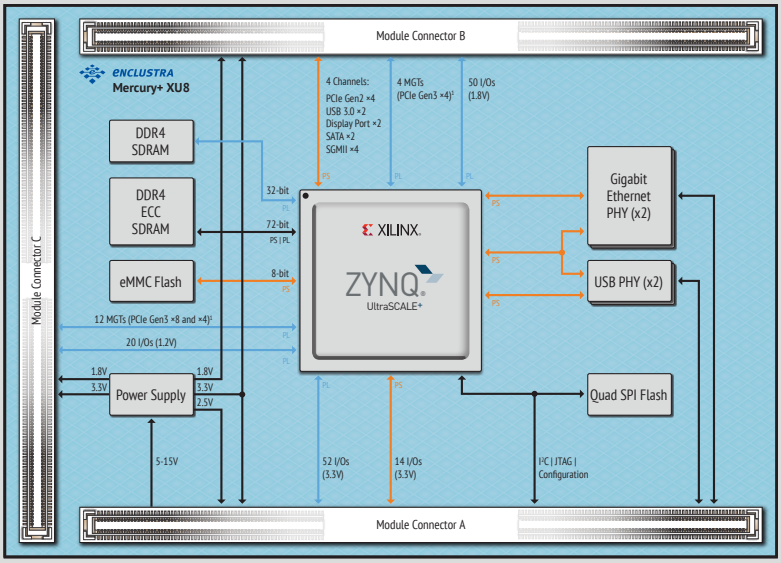


MERCURY+ XU8

Zynq® UltraScale+™ SoC Module

OS support:

- Xilinx® Zynq UltraScale+ MPSoC
- ZU4CG/ZU5EV/ZU7EV devices
- Dual-/Quad-core ARM® Cortex™-A53
- Dual-core ARM Cortex-R5
- H.264/H.265 Video Codec (EV only)
- Up to 8 GB DDR4 ECC SDRAM (PS side)
- Up to 4 GB DDR4 SDRAM (PL side)
- 16 GB eMMC flash
- 64 MB QSPI flash
- PCIe® Gen3 × 16 and PCIe Gen2 × 4
- 20 × 6/12.5/15 Gbps MGT
- 2 × Gigabit Ethernet
- 2 × USB 2.0/3.0
- Up to 504,000 system logic cells
- 236 user I/Os
- 5–15 V supply
- 74 × 54 mm



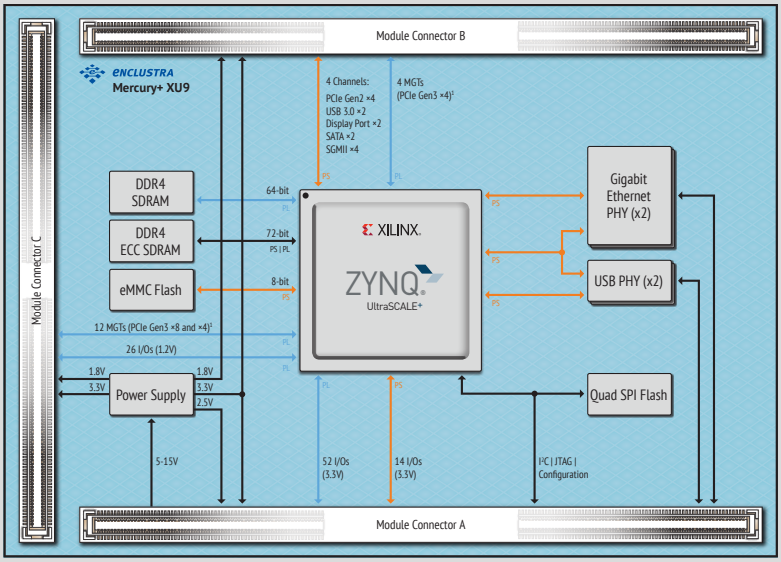
1: PCIe Gen3 ×16 available at the system level by merging the MGTs from connectors B and C.

MERCURY+ XU9

Zynq® UltraScale+™ SoC Module

OS support:

- Xilinx® Zynq UltraScale+ MPSoC
- ZU4CG/ZU5EV/ZU7EV devices
- Dual-/Quad-core ARM® Cortex™-A53
- Dual-core ARM Cortex-R5
- H.264 / H.265 Video Codec (EV only)
- Up to 8 GB DDR4 ECC SDRAM (PS side)
- Up to 8 GB DDR4 SDRAM (PL side)
- 16 GB eMMC flash
- 64 MB QSPI flash
- 20 × 6/12.5/15 Gbps MGT
- PCIe® Gen3 × 16 and PCIe Gen2 × 4
- 2 × Gigabit Ethernet
- 2 × USB 2.0/3.0
- Up to 504,000 system logic cells
- 192 user I/Os
- 5–15 V supply
- 74 × 54 mm



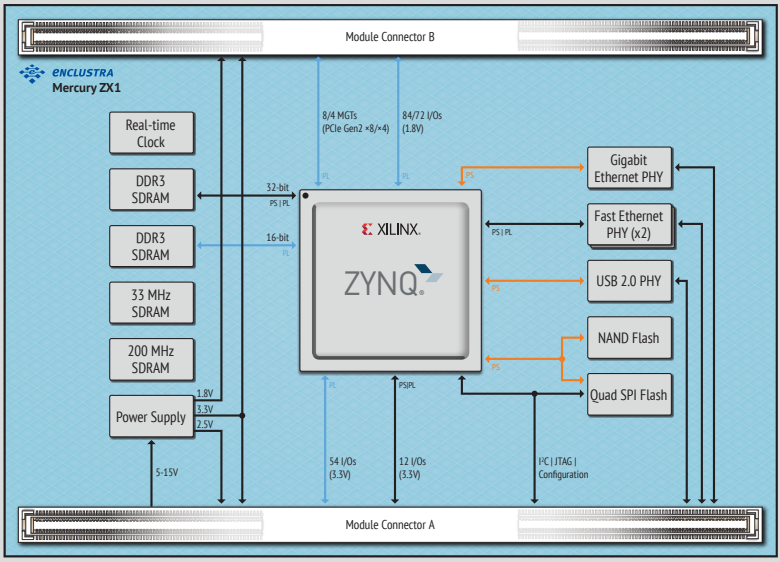
1: PCIe Gen3 ×16 available at the system level by merging the MGTs from connectors B and C.

MERCURY ZX1

Zynq®-7030/7035/7045 SoC Module

OS support:

- Xilinx® Zynq-7030/7035/7045 SoC FPGA
- Dual-core ARM® Cortex™-A9
- 1 GB + 256 MB DDR3L SDRAM
- 64 MB QSPI flash
- 512 MB NAND flash
- PCIe® Gen2 × 4/ × 8
- Up to 8 × 6.6/10.3125 Gbps MGT
- Gigabit Ethernet
- 2 × Fast Ethernet
- USB 2.0 OTG
- Up to 350,000 system logic cells
- Up to 178 user I/Os
- 5–15 V supply
- 64 × 54 mm

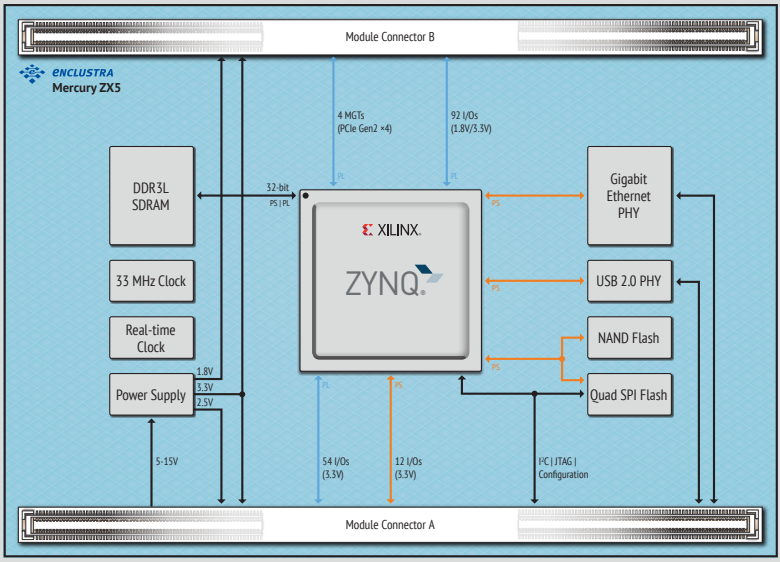


MERCURY ZX5

Zynq®-7015/7030 SoC Module

OS support:

- Xilinx® Zynq-7015/7030 SoC FPGA
- Dual-core ARM® Cortex™-A9
- 1 GB DDR3L SDRAM
- 64 MB QSPI flash
- 512 MB NAND flash
- PCIe® Gen2 × 4
- 4 × 6.25/6.6 Gbps MGT
- Gigabit Ethernet
- USB 2.0 OTG
- Up to 125,000 system logic cells
- 178 user I/Os
- 5–15 V supply
- 56 × 54 mm

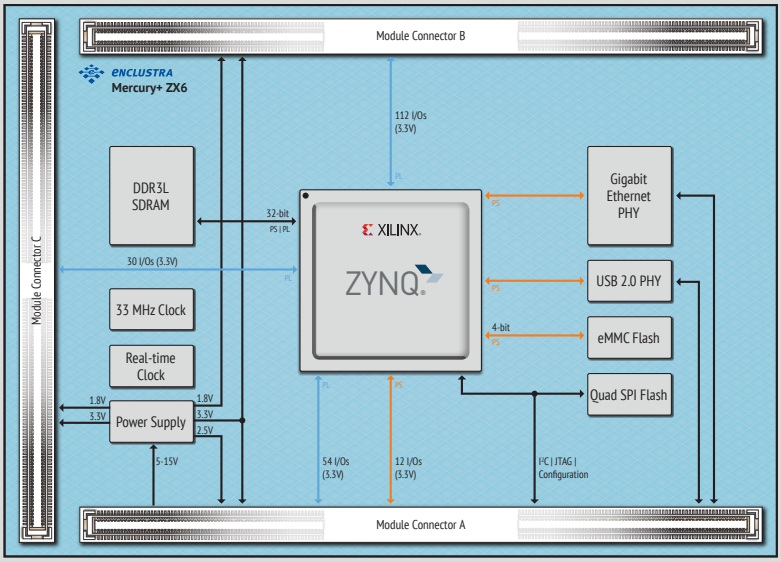


MERCURY+ ZX6

Zynq®-7014S/7020 SoC Module

OS support:

- Xilinx® Zynq-7014S/7020 SoC FPGA
- Single-/Dual-core ARM Cortex-A9
- Up to 1 GB DDR3L SDRAM
- 16 GB eMMC flash
- 64 MB QSPI flash
- Gigabit Ethernet
- USB 2.0 OTG
- Up to 85,000 system logic cells
- 208 user I/Os
- 5–15 V supply
- 65 × 54 mm

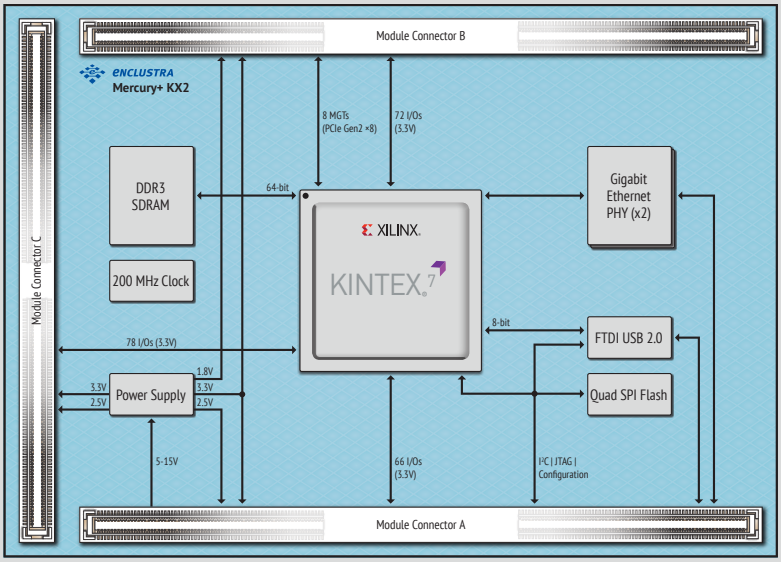


Concept – we are actively looking for customers interested in this or a similar module. Please contact us with your detailed requirements.

MERCURY+ KX2

Kintex®-7 FPGA Module

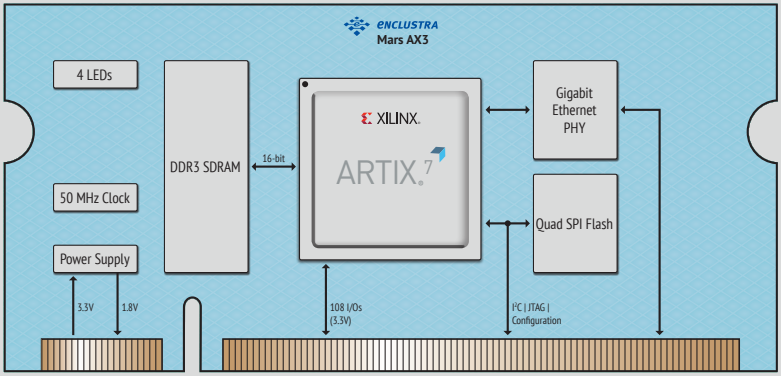
- Xilinx® Kintex-7 FPGA
- Up to 4 GB DDR3L SDRAM
- 64 MB QSPI flash
- PCIe® Gen2 × 8
- 8 × 6.6/10.3125 Gbps MGT
- USB 2.0 device controller
- 2 × Gigabit Ethernet
- Up to 407,000 system logic cells
- 256 user I/Os
- 5–15 V single supply
- 74 × 54 mm



MARS AX3

Artix®-7 FPGA Module

- Xilinx® Artix-7 FPGA
- Up to 512 MB DDR3L SDRAM
- 64 MB QSPI flash
- Gigabit Ethernet
- Up to 101,440 system logic cells
- 108 user I/Os
- 3.3 V single supply
- 67.6 × 30 mm SO-DIMM

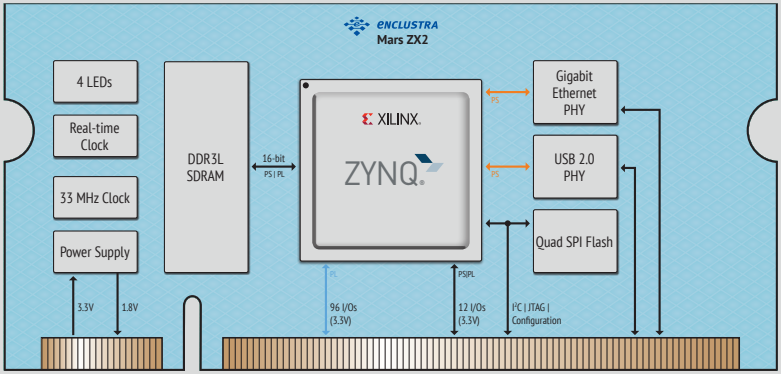


MARS ZX2

Zynq®-7010/7020 SoC Module

OS support:

- Xilinx® Zynq-7010/7020 SoC FPGA
- Dual-core ARM® Cortex™-A9
- 512 MB DDR3L SDRAM
- 64 MB QSPI flash
- USB 2.0 OTG
- Gigabit Ethernet
- Up to 85,000 system logic cells
- 108 user I/Os
- 3.3 V single supply
- 67.6 × 30 mm SO-DIMM

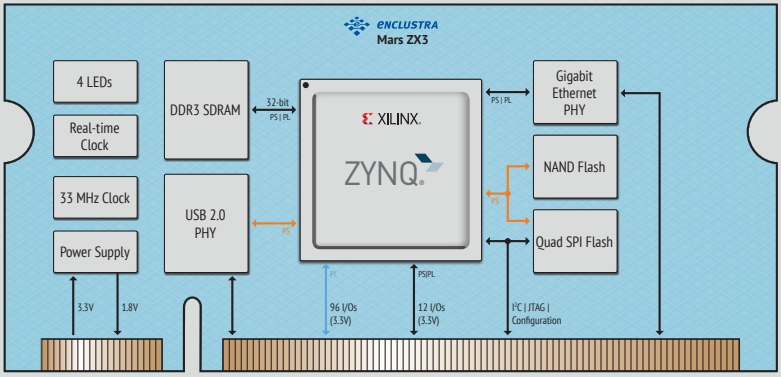


MARS ZX3

Zynq®-7020 SoC Module

OS support:

- Xilinx® Zynq-7020 SoC FPGA
- Dual-core ARM® Cortex™-A9
- Up to 1 GB DDR3L SDRAM
- 64 MB QSPI flash
- 512 MB NAND flash
- USB 2.0 OTG
- Gigabit Ethernet
- Up to 85,000 system logic cells
- 108 user I/Os
- 3.3 V single supply
- 67.6 × 30 mm SO-DIMM

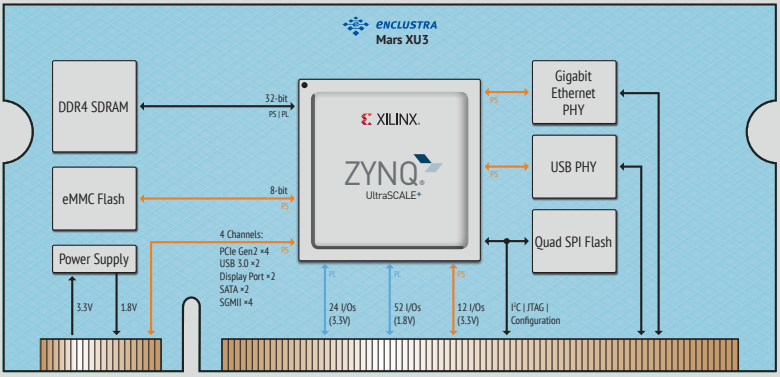


MARS XU3

Zynq® UltraScale+™ SoC Module

OS support:

- Xilinx® Zynq UltraScale+ MPSoC
- ZU2CG/ZU2EG/ZU3EG devices
- Dual-/Quad-core ARM® Cortex™-A53
- Up to 4 GB DDR4 SDRAM
- 16 GB eMMC flash
- 64 MB QSPI flash
- PCIe® Gen2 × 4
- 4 × 5 Gbps MGT
- Gigabit Ethernet
- USB 3.0
- USB 2.0 OTG
- Up to 154,000 system logic cells
- 108 user I/Os
- 67.6 × 30 mm SO-DIMM

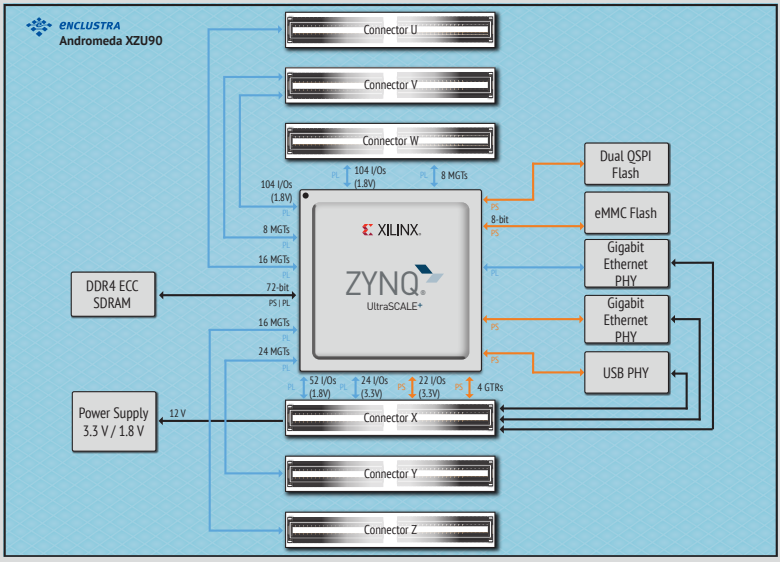


ANDROMEDA XZU90

Zynq® UltraScale+™ SoC Module

OS support:

- Xilinx® Zynq UltraScale+ MPSoC
- ZU17EG/ZU19EG devices
- Quad-core ARM® Cortex™-A53
- Dual-core ARM Cortex-R5
- Up to 8 GB DDR4 SDRAM (PS side)
- 16 GB eMMC flash
- 128 MB QSPI flash dual-parallel
- 76 × 6/16.3/25 Gbps MGT
- Up to 5 × PCIe® Gen3 × 16 and PCIe Gen2 × 4
- 2 × Gigabit Ethernet
- USB 2.0/3.0
- Up to 1,143,000 system logic cells
- 686 user I/Os
- 12 V supply
- 80 × 64 mm

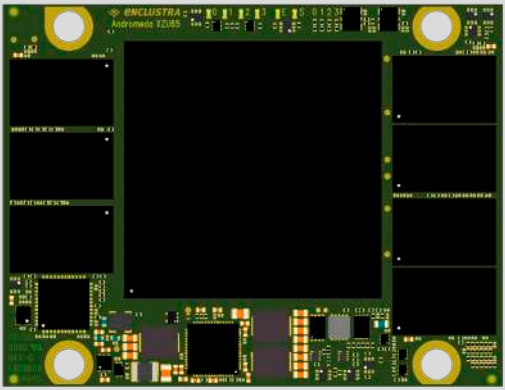


Early Access – please contact us for availability.

ANDROMEDA XZU65

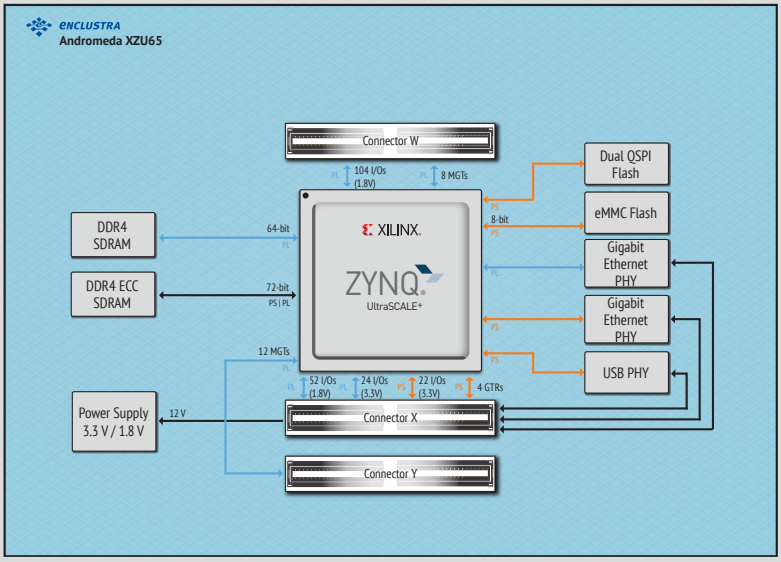
Zynq® UltraScale+™ SoC Module

OS support:



Rendering

- Xilinx® Zynq UltraScale+ MPSoC
- ZU7EG/ZU7EV/ZU11EG devices
- Quad-core ARM® Cortex™-A53
- Dual-core ARM Cortex-R5
- H.264 / H.265 Video Codec (EV only)
- Up to 8 GB DDR4 SDRAM (PS side)
- Up to 8 GB DDR4 SDRAM (PL side)
- 16 GB eMMC flash
- 128 MB QSPI flash dual-parallel
- 24 × 6/16.3 Gbps MGT
- PCIe® Gen3 × 16 and PCIe Gen2 × 4
- 2 × Gigabit Ethernet
- USB 2.0/3.0
- Up to 653,100 system logic cells
- 322 user I/Os
- 12 V supply
- 68 × 52 mm



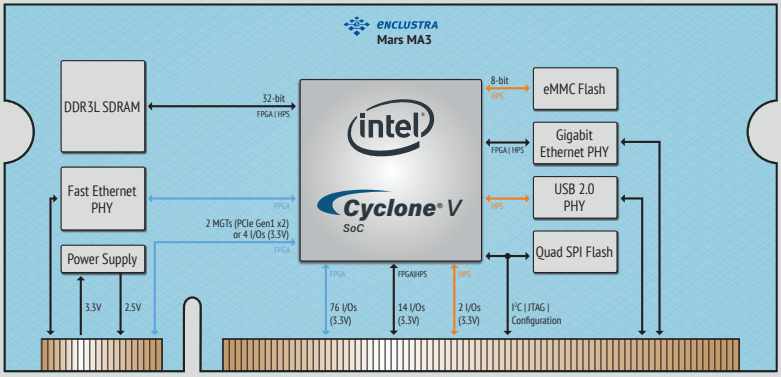
In development – please contact us for availability.

MARS MA3

Cyclone® V SoC Module

OS support:

- Intel® Cyclone V SoC
- Dual-core ARM® Cortex™-A9
- Up to 2 GB DDR3L SDRAM
- 16 GB eMMC flash
- 64 MB QSPI flash
- PCIe® Gen1 × 2
- 3.125 Gpbs MGT
- Gigabit Ethernet, Fast Ethernet
- USB 2.0 OTG
- 110,000 system logic elements
- 104 user I/Os
- 3.3 V single supply
- 67.6 × 30 mm SO-DIMM

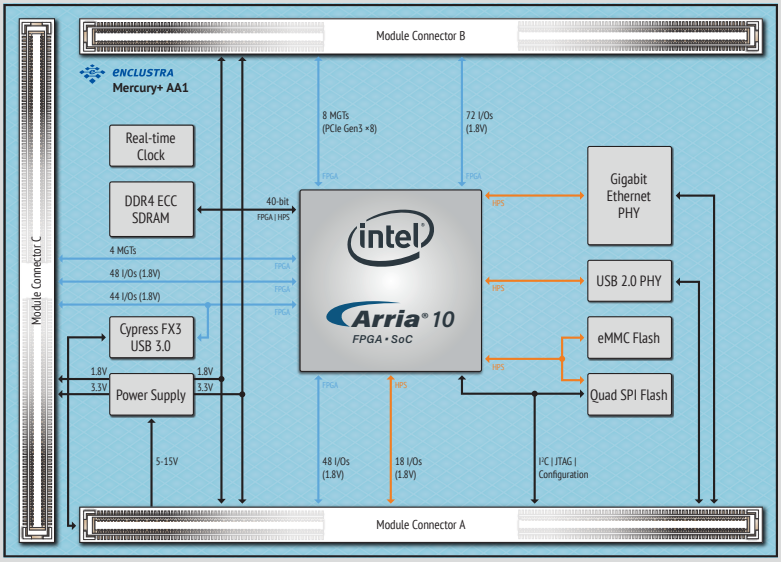


MERCURY+ AA1

Arria® 10 SoC Module

OS support:

- Intel® Arria 10 SoC
- Dual-core ARM® Cortex™-A9
- Up to 4 GB DDR4 ECC SDRAM
- 64 MB QSPI flash
- 16 GB eMMC flash
- PCIe® Gen3 × 8, PCIe® Gen3 × 4
- 12 × 10.3125/12.5 Gbps MGT
- USB 3.0 device controller
- USB 2.0 host/device
- Gigabit Ethernet
- Up to 480,000 system logic elements
- 286 user I/Os
- 5–15 V supply
- 74 × 54 mm

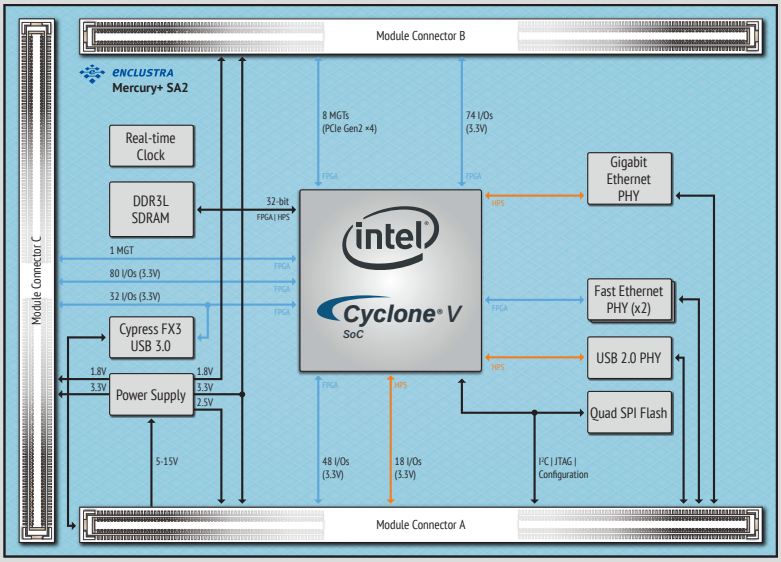


MERCURY+ SA2

Cyclone® V SoC Module

OS support:

- Intel® Cyclone V SoC
- Dual-core ARM® Cortex™-A9
- Up to 4 GB DDR3L SDRAM
- 64 MB QSPI flash
- PCIe® Gen1/Gen2 × 4
- 9 × 3.125/6.144 Gbps MGT
- USB 3.0 device controller
- USB 2.0 host/device
- Gigabit Ethernet, 2 × Fast Ethernet
- Up to 110,000 system logic elements
- 294 user I/Os
- 5–15 V supply
- 74 × 54 mm

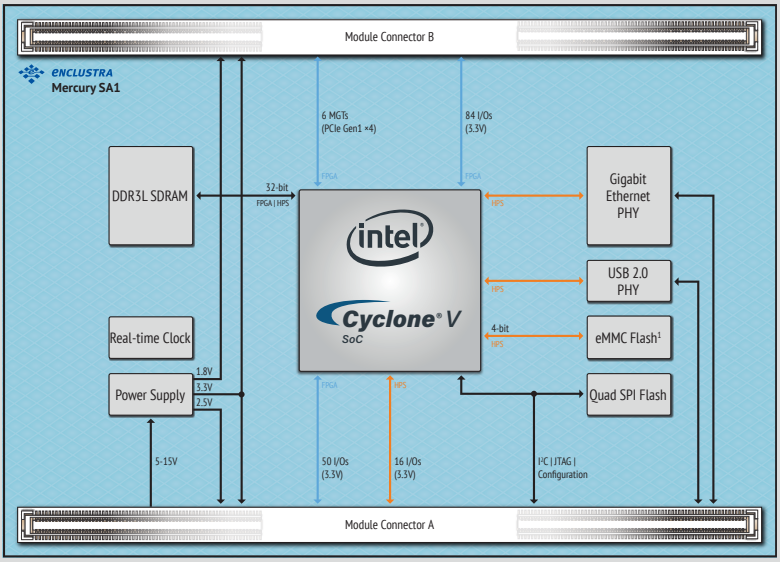


MERCURY SA1

Cyclone® V SoC Module

OS support:

- Intel® Cyclone V SoC FPGA
- Dual-core ARM® Cortex™-A9
- Up to 4 GB DDR3L SDRAM
- 64 MB QSPI flash
- 16 GB eMMC flash
- PCIe® Gen1 × 4
- 6 × 3.125 Gbps MGT
- USB 2.0 OTG
- Gigabit Ethernet
- 110,000 system logic elements
- 178 user I/Os
- 5–15 V supply
- 56 × 54 mm

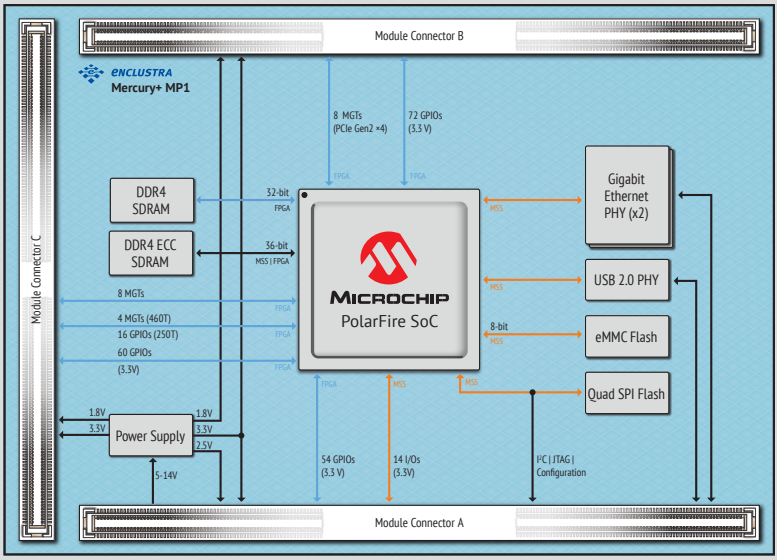


MERCURY+ MP1

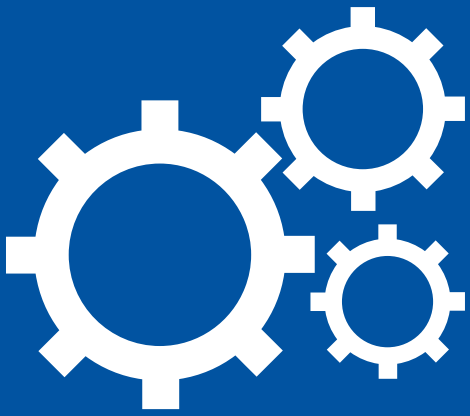
PolarFire™ SoC Module

OS support:

- Microchip® PolarFire SoC
- MPFS250T/MPFS460T devices
- RISC-V RV64CG Quad-core
- RISC-V RV64IMAC Monitor core
- Crypto Co-processor
- Up to 4 GB ECC DDR4 SDRAM (MSS side)
- Up to 4 GB DDR4 SDRAM (FPGA fabric side)
- 64 MB QSPI flash (MSS)
- 64 MB SPI flash (FPGA fabric)
- 16 GB eMMC flash
- Up to 20 × up to 12.7 Gbps MGT
- 2 × Gigabit Ethernet (MSS)
- USB 2.0 OTG
- Up to 461,000 logic elements
- 294 user I/Os
- 5–14 V supply
- 74 × 54 mm



In development – please contact us for availability.



Need some tweaks?

If you find that one of our modules almost meets your needs, but you have different interfacing or device needs, let us know – we frequently customize our products to specific requirements.

Valid as of October 5th 2021. Consult the product web pages for a full listing of available models.	Mars™ ZX2		Mars™ ZX3		Mars™ XU3		
FPGA Family	Zynq®-7000		Zynq®-7000		Zynq® UltraScale+™		
FPGA Device Name	Z-7010	Z-7020	Z-7020		ZU2CG	ZU2EG	ZU3EG
FPGA Speed Grade*2	2	2	1	2	1	1	2
FPGA Part Number*2	XC7Z010-2CLG400I	XC7Z020-2CLG400I	XC7Z020-1CLG484C	XC7Z020-2CLG484I	XCZU2CG-1SBVA484E	XCZU2EG-1SBVA484I	XCZU3EG-2SBVA484I
CPU Cores	2 x ARM® Cortex™-A9		2 x ARM® Cortex™-A9		2 x A53 | 2 x R5	4 x ARM® Cortex™-A53 | 2 x Cortex™-R5	
CPU Frequency @ MHz	766		667	766	1,200 | 500		1,333 | 533
PS Peripherals	2 x CAN		2 x CAN		DP | PCIe® Gen2 x4 SATA | SGMII | CAN	Mali™ | DisplayPort | PCIe® Gen2 x4 SATA | SGMII | CAN	
PS Ethernet | USB	1 Gbps | USB 2.0 OTG		1 Gbps | USB 2.0 OTG		1 Gbps | USB 3.0		
PS SDRAM Size (MByte)	512		512	1,024	1,024		2,048
PS SDRAM Type | Bandwidth (MByte/s)	DDR3L | 2,132		DDR3L | 4,264		DDR4 | 4,264		
PL System Logic Cells	28'160	85'120	85'120		103'000		154'000
PL Block RAM (kbit)	2'160	5'040	5'040		5'400		7'776
PL DSP Systolic FIR (GMAC/s)	88	242	204	242	310		558
PL MGT Transceivers @ Gbps*6	-		-		-		
PL Peripherals	-		-		-		
PL Ethernet | USB*5	-		1 Gbps		-		
PL SDRAM Size (MByte)	-		-		-		
PL SDRAM Type | Bandwidth (MByte/s)	-		-		-		
Flash Memory	64M QSPI		64M QSPI | 512M NAND		64M QSPI | 16G eMMC		
Connector Pins | IO Pins	200 | 108		200 | 108		200 | 108		
PL 3.3V | PL 1.8V | PL 1.2V Pins | PS Pins	96 | - | - | 12	108 | - | - | 12	108 | - | - | 12		24 | 52 | - | 12		
Module Dimensions (mm)	67.6 x 30		67.6 x 30		67.6 x 30		
Temperature Range*2	-40..+85°C		0..+70°C	-40..+85°C	0..+85°C	-40..+85°C	
Boot Modes	QSPI | SD Card		QSPI | SD Card		QSPI | SD Card | eMMC		
Product Status	Active		Active		Active		
Estimated Product Lifetime*3	2030+		2030+		2030+		
Preferred Model | MOQ*4	Yes	Yes	Yes	Yes	Yes	No | 70	Yes
Product Model	MA-ZX2-10-2I-D9	MA-ZX2-20-2I-D9	MA-ZX3-20-1C-D9	MA-ZX3-20-2I-D10	MA-XU3-2CG-1E-D10	MA-XU3-2EG-1I-D10	MA-XU3-3EG-2I-D11

*** Notes**

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2. The module is also available in different speed and temperature grades. Visit the product web page for more information.
3. Please contact us about production data backup and module production license options.
4. For non-preferred models, the minimum order quantity (MOQ) only applies if the modules are not in stock – contact us for more details.
5. Check out our FPGA Manager IP solution for simple data streaming into Windows/Linux embedded/host PCs.
6. Please ensure that adequate signal integrity is obtained over the full signal path when using MGT's at high performance.

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Valid as of October 5th 2021. Consult the product web pages for a full listing of available models.	Mars™ AX3			Mercury+™ KX2	
FPGA Family	Artix®-7			Kintex®-7	
FPGA Device Name	35	50	100	160T	410T
FPGA Speed Grade*2	1	1	2	1	2
FPGA Part Number*2	XC7A35T-1CSG324I	XC7A50T-1CSG324I	XC7A100T-2CSG324I	XC7K160T-1FBG676C	XC7K410T-2FFG676I
CPU Cores	-			-	
CPU Frequency @ MHz	-			-	
PS Peripherals	-			-	
PS Ethernet | USB	-			-	
PS SDRAM Size (MByte)	-			-	
PS SDRAM Type | Bandwidth (MByte/s)	-			-	
PL System Logic Cells	33'280	52'160	101'440	162'240	406'720
PL Block RAM (kbit)	1'800	2'700	4'860	11'700	28'620
PL DSP Systolic FIR (GMAC/s)	84	111	264	780	2'002
PL MGT Transceivers @ Gbps*6	-			8 @ 10.3125	
PL Peripherals	-			PCIe® Gen2 x8	
PL Ethernet | USB*5	1 Gbps			2 x 1 Gbps | FTDI USB 2.0	
PL SDRAM Size (MByte)	256			2'048	
PL SDRAM Type | Bandwidth (MByte/s)	DDR3 | 1,600			DDR3L | 12,800	
Flash Memory	64M QSPI			64M QSPI	
Connector Pins | IO Pins	200 | 108			504 | 256	
PL 3.3V | PL 1.8V | PL 1.2V Pins | PS Pins	108 | - | - | -			216 | - | - | -	
Module Dimensions (mm)	67.6 x 30			74 x 54	
Temperature Range*2	-40..+85°C			-40..+85°C	
Boot Modes	Slave Serial | QSPI			Slave Serial | QSPI | USB2	
Product Status	Active			Active	
Estimated Product Lifetime*3	2030+			2030+	
Preferred Model | MOQ*4	Yes	No | 90	Yes	Yes	No | 20
Product Model	MA-AX3-35-1I-D8	MA-AX3-50-1I-D8	MA-AX3-100-2I-D8	ME-KX2-160-2I-D11-P	ME-KX2-410-2I-D11-P

*** Notes**
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Valid as of October 5th 2021. Consult the product web pages for a full listing of available models.	Mercury™ ZX1			Mercury™ ZX5			Mercury+™ ZX6	
FPGA Family	Zynq®-7000			Zynq®-7000			Zynq®-7000	
FPGA Device Name	Z-7030	Z-7035	Z-7045	Z-7015	Z-7030		Z-7014S	Z-7020
FPGA Speed Grade*2	2	1	2	2	1	3	1	2
FPGA Part Number*2	XC7Z030-2FBG676I	XC7Z035-1FBG676I	XC7Z045-2FFG676I	XC7Z015-2CLG485I	XC7Z030-1SBG485I	XC7Z030-3SBG485E	XC7Z014S-1CLG484C	XC7Z020-2CLG484I
CPU Cores	2 x ARM® Cortex™-A9			2 x ARM® Cortex™-A9			ARM® Cortex™-A9	2 x ARM® Cortex™-A9
CPU Frequency @ MHz	800	667	800	766	667	1'000	667	766
PS Peripherals	2 x CAN			2 x CAN			2 x CAN	
PS Ethernet | USB	1 Gbps | USB 2.0 OTG			1 Gbps | USB 2.0 OTG			1 Gbps | USB 2.0 OTG	
PS SDRAM Size (MByte)	1,024			1,024			512	1,024
PS SDRAM Type | Bandwidth (MByte/s)	DDR3L | 4,264			DDR3L | 4,264		DDR3L | 5,333	DDR3L | 4,264	
PL System Logic Cells	125'000	275'000	350'000	73'920	125'000		64'960	85'120
PL Block RAM (kbit)	9'540	18'000	19'620	3'420	9'540		3'852	5'040
PL DSP Systolic FIR (GMAC/s)	520	981	1'170	176	438	593	158	242
PL MGT Transceivers @ Gbps*6	4 @ 6.6	8 @ 6.6	8 @ 10.3125	4 @ 6.25	4 @ 6.6		-	
PL Peripherals	PCIe® Gen2 x4	PCIe® Gen2 x8		PCIe® Gen2 x4			-	
PL Ethernet | USB*5	2 x 100 Mbps			-			-	
PL SDRAM Size (MByte)	256			-			-	
PL SDRAM Type | Bandwidth (MByte/s)	DDR3L | 2,133	DDR3L | 1,600	DDR3L | 3,200	-			-	
Flash Memory	64M QSPI | 512M NAND			64M QSPI | 512M NAND			64M QSPI | 16G eMMC	
Connector Pins | IO Pins	336 | 170	336 | 178		336 | 178			504 | 208	
PL 3.3V | PL 1.8V | PL 1.2V Pins | PS Pins	66 | 84 | - | 12	66 | 72 | - | 12		146 | - | - | 12	54 | 92 | - | 12		196 | - | - | 12	
Module Dimensions (mm)	64 x 54			56 x 54			65 x 54	
Temperature Range*2	-40..+85°C			-40..+85°C		0..+70°C	0..+70°C	-40..+85°C
Boot Modes	QSPI | SD Card | NAND			QSPI | SD Card | NAND			QSPI | SD Card	
Product Status	Active			Active			Concept*1	
Estimated Product Lifetime*3	2030+			2030+			2030+	
Preferred Model | MOQ*4	Yes	Yes	Yes	Yes	Yes	No | 40	TBD	
Product Model	ME-ZX1-30-2I-D10	ME-ZX1-35-1I-D10	ME-ZX1-45-2I-D10-P	ME-ZX5-15-2I-D10	ME-ZX5-30-1I-D10	ME-ZX5-30-3C-D10	ME-ZX6-14S-1C-D9	ME-ZX6-20-2I-D10

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Valid as of October 5th 2021. Consult the product web pages for a full listing of available models.	Mercury+™ XU1					Mercury+™ XU1 (cont.)					
FPGA Family	Zynq® UltraScale+™					Zynq® UltraScale+™					
FPGA Device Name	ZU6CG		ZU6EG		ZU9EG	ZU9EG		ZU9EG	ZU15EG	ZU15EG	
FPGA Speed Grade*2	1		1		1	2		3	1	2	
FPGA Part Number*2	XCZU6CG-1FFVC900E		XCZU6EG-1FFVC900I		XCZU9EG-1FFVC900E	XCZU9EG-2FFVC900I		XCZU9EG-3FFVC900E	XCZU15EG-1FFVC900E	XCZU15EG-2FFVC900I	
CPU Cores	2 x A53 | 2 x R5		4 x ARM® Cortex™-A53 | 2 x Cortex™-R5			4 x ARM® Cortex™-A53 | 2 x Cortex™-R5					
CPU Frequency @ MHz	1,200 | 500					1,333 | 533		1,500 | 600	1,200 | 500	1,333 | 533	
PS Peripherals	DisplayPort | PCIe® Gen2 x4 SATA | SGMII | CAN		Mali™ | DisplayPort | PCIe® Gen2 x4 SATA | SGMII | CAN			Mali™ | DisplayPort | PCIe® Gen2 x4 SATA | SGMII | CAN					
PS Ethernet | USB	2 x 1 Gbps | 2 x USB 3.0					2 x 1 Gbps | 2 x USB 3.0					
PS SDRAM Size (MByte)	2,048 + ECC					4,096 + ECC					
PS SDRAM Type | Bandwidth (MByte/s)	DDR4 | 19,200					DDR4 | 19,200					
PL System Logic Cells	469'446				599'550	599'550			746'550		
PL Block RAM (kbit)	25'704				32'832	32'832			59'040		
PL DSP Systolic FIR (GMAC/s)	2'545				3'251	3'906		4'491	4'551	5'468	
PL MGT Transceivers @ Gbps*6	16 @ 12.5	12 @ 12.5	16 @ 12.5	12 @ 12.5	16 @ 12.5	12 @ 15	16 @ 15	12 @ 15	16 @ 12.5	12 @ 15	16 @ 15
PL Peripherals	-					-					
PL Ethernet | USB*5	-					-					
PL SDRAM Size (MByte)	-					-					
PL SDRAM Type | Bandwidth (MByte/s)	-					-					
Flash Memory	64M QSPI | 16G eMMC					64M QSPI | 16G eMMC					
Connector Pins | IO Pins	504 | 294					504 | 294					
PL 3.3V | PL 1.8V | PL 1.2V Pins | PS Pins	52 | 128 | - | 14	52 | 148 | - | 14	52 | 128 | - | 14	52 | 148 | - | 14	52 | 128 | - | 14	52 | 148 | - | 14	52 | 128 | - | 14	52 | 148 | - | 14	52 | 128 | - | 14	52 | 148 | - | 14	52 | 128 | - | 14
Module Dimensions (mm)	74 x 54					74 x 54					
Temperature Range*2	0..+85°C		-40..+85°C		0..+85°C	-40..+85°C		0..+85°C		-40..+85°C	
Boot Modes	QSPI | SD Card | eMMC					QSPI | SD Card | eMMC					
Product Status	Active					Active					
Estimated Product Lifetime*3	2030+					2030+					
Preferred Model | MOQ*4	Yes	No | 30	No | 20	Yes	No | 20	No | 20	No | 20	No | 20	Yes	Yes	No | 20
Product Model	ME-XU1-6CG-1E-D11E-G1	ME-XU1-6CG-1E-D11E	ME-XU1-6EG-1I-D11E-G1	ME-XU1-6EG-1I-D11E	ME-XU1-9EG-1E-D11E-G1	ME-XU1-9EG-2I-D12E	ME-XU1-9EG-2I-D12E-G1	ME-XU1-9EG-3E-D12E	ME-XU1-15EG-1E-D12E-G1	ME-XU1-15EG-2I-D12E	ME-XU1-15EG-2I-D12E-G1

*** Notes**

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Valid as of October 5th 2021. Consult the product web pages for a full listing of available models.	Mercury™ XU5				Mercury™ XU5 (cont.)					
FPGA Family	Zynq® UltraScale+™				Zynq® UltraScale+™					
FPGA Device Name	ZU2CG	ZU2EG	ZU3EG	ZU4CG	ZU4EV	ZU4EV	ZU5EV	ZU5EV	ZU5EV	ZU5EV
FPGA Speed Grade*2	1	1	2	1	1	1	1	2	2	3
FPGA Part Number*2	XCZU2CG-1SFVC784E	XCZU2EG-1SFVC784I	XCZU3EG-2SFVC784I	XCZU4CG-1SFVC784E	XCZU4EV-1SFVC784I	XCZU4EV-1SFVC784I	XCZU5EV-1SFVC784E	XCZU5EV-2SFVC784I	XCZU5EV-2SFVC784I	XCZU5EV-3SFVC784E
CPU Cores	2 x ARM® Cortex™-A53 2 x Cortex™-R5	4 x ARM® Cortex™-A53 2 x Cortex™-R5		2 x ARM® Cortex™-A53 2 x Cortex™-R5	4 x ARM® Cortex™-A53 | 2 x Cortex™-R5					
CPU Frequency @ MHz	1,200 | 500		1,333 | 533	1,200 | 500	1,200 | 500			1,333 | 533		1,500 | 600
PS Peripherals	DP | PCIe® Gen2 x4 SATA | SGMII | CAN	Mali™ | DP | PCIe® Gen2 x4 SATA | SGMII | CAN		CAN	Mali™ | DP | PCIe® Gen2 x4 SATA | SGMII | CAN	Mali™ | CAN	Mali™ | DP | PCIe® Gen2 x4 SATA | SGMII | CAN		Mali™ | CAN	Mali™ | DP | PCIe® Gen2 x4 SATA | SGMII | CAN
PS Ethernet | USB	1 Gbps | 2 x USB 3.0			1 Gbps | 2 x USB 2.0	1 Gbps | 2 x USB 3.0	1 Gbps | 2 x USB 2.0	1 Gbps | 2 x USB 3.0		1 Gbps | 2 x USB 2.0	1 Gbps | 2 x USB 3.0
PS SDRAM Size (MByte)	1,024	2,048 + ECC			2,048 + ECC		4,096 + ECC			8,192 + ECC
PS SDRAM Type | Bandwidth (MByte/s)	DDR4 | 9,600	DDR4 | 19,200			DDR4 | 19,200					
PL System Logic Cells	103'320		154'350	192'150	192'150		256'200			
PL Block RAM (kbit)	5'400		7'776	18'432	18'432		23'616			
PL DSP Systolic FIR (GMAC/s)	310		558	939	939		1'610	1'934		2'224
PL MGT Transceivers @ Gbps*6	-			4 @ 12.5	4 @ 12.5					
PL Peripherals	-			PCIe® Gen3 x4	H.265 Codec PCIe® Gen3 x4					
PL Ethernet | USB*5	1 Gbps				1 Gbps					
PL SDRAM Size (MByte)	512				512			1,024		2,048
PL SDRAM Type | Bandwidth (MByte/s)	DDR4 | 4,266		DDR4 | 4,800	DDR4 | 4,266	DDR4 | 4,266			DDR4 | 4,800		
Flash Memory	64M QSPI | 16G eMMC				64M QSPI | 16G eMMC					
Connector Pins | IO Pins	336 | 178				336 | 178					
PL 3.3V | PL 1.8V | PL 1.2V Pins | PS Pins	52 | 92 | - | 14			54 | 92 | - | 12	52 | 72 | - | 14	54 | 92 | - | 12	52 | 72 | - | 14		54 | 92 | - | 12	52 | 72 | - | 14
Module Dimensions (mm)	56 x 54				56 x 54					
Temperature Range*2	0..+85°C	-40..+85°C		0..+85°C	-40..+85°C		0..+85°C	-40..+85°C		0..+85°C
Boot Modes	QSPI | SD Card | eMMC				QSPI | SD Card | eMMC					
Product Status	Active				Active					
Estimated Product Lifetime*3	2030+				2030+					
Preferred Model | MOQ*4	Yes	Yes	Yes	No | 50	Yes	Yes	No | 30	Yes	No | 30	No | 20
Product Model	ME-XU5-2CG-1E-D10H	ME-XU5-2EG-1I-D11E	ME-XU5-3EG-2I-D11E	ME-XU5-4CG-1E-D11E-G1	ME-XU5-4EV-1I-D11E	ME-XU5-4EV-1I-D11E-G1	ME-XU5-5EV-1E-D11E	ME-XU5-5EV-2I-D12E	ME-XU5-5EV-2I-D12E-G1	ME-XU5-5EV-3E-D13E

*** Notes**

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Valid as of October 5th 2021. Consult the product web pages for a full listing of available models.	Mercury+™ XU7			Mercury+™ XU8			
FPGA Family	Zynq® UltraScale+™			Zynq® UltraScale+™			
FPGA Device Name	ZU6EG	ZU9EG	ZU15EG	ZU4CG	ZU5EV	ZU7EV	
FPGA Speed Grade*2	1	2	2	1	1	1	2
FPGA Part Number*2	XCZU6EG-1FFVC900I	XCZU9EG-2FFVC900I	XCZU15EG-2FFVC900I	XCZU4CG-1FBVB900E	XCZU5EV-1FBVB900I	XCZU7EV-1FBVB900E	XCZU7EV-2FBVB900I
CPU Cores	4 x ARM® Cortex™-A53 | 2 x Cortex™-R5			2 x A53 | 2 x R5	4 x ARM® Cortex™-A53 | 2 x Cortex™-R5		
CPU Frequency @ MHz	1,200 | 500	1,333 | 533		1,200 | 500			1,333 | 533
PS Peripherals	Mali™ | DisplayPort | PCIe® Gen2 x4 SATA | SGMII | CAN			DP | PCIe® Gen2 x4 SATA | SGMII | CAN	Mali™ | DisplayPort | PCIe® Gen2 x4 SATA | SGMII | CAN		
PS Ethernet | USB	2 x 1 Gbps | 2 x USB 3.0			2 x 1 Gbps | 2 x USB 3.0			
PS SDRAM Size (MByte)	2,048 + ECC	4,096 + ECC		2,048 + ECC	4,096 + ECC	2,048 + ECC	4,096 + ECC
PS SDRAM Type | Bandwidth (MByte/s)	DDR4 | 19,200			DDR4 | 19,200			
PL System Logic Cells	469'446	599'550	746'550	192'150	256'200	504'000	
PL Block RAM (kbit)	25'704	32'832	59'040	18'432	23'616	38'880	
PL DSP Systolic FIR (GMAC/s)	2'545	3'906	5'468	939	1'610	2'229	2'678
PL MGT Transceivers @ Gbps*6	16 @ 12.5	16 @ 15		16 @ 12.5			16 @ 15
PL Peripherals	-			PCIe® Gen3 x16	PCIe® Gen3 x16 | H.265 Codec		
PL Ethernet | USB*5	-			-			
PL SDRAM Size (MByte)	1'024	2'048		1'024	2'048	1'024	2'048
PL SDRAM Type | Bandwidth (MByte/s)	DDR4 | 9,600			DDR4 | 9,600			
Flash Memory	64M QSPI | 16G eMMC			64M QSPI | 16G eMMC			
Connector Pins | IO Pins	504 | 236			504 | 236			
PL 3.3V | PL 1.8V | PL 1.2V Pins | PS Pins	52 | 50 | 20 | 14			52 | 50 | 20 | 14			
Module Dimensions (mm)	74 x 54			74 x 54			
Temperature Range*2	-40..+85°C			0..+85°C	-40..+85°C	0..+85°C	-40..+85°C
Boot Modes	QSPI | SD Card | eMMC			QSPI | SD Card | eMMC			
Product Status	Active			Active			
Estimated Product Lifetime*3	2030+			2030+			
Preferred Model | MOQ*4	Yes	No | 20	Yes	Yes	No | 20	No | 20	Yes
Product Model	ME-XU7-6EG-1I-D11E	ME-XU7-9EG-2I-D12E	ME-XU7-15EG-2I-D12E	ME-XU8-4CG-1E-D11E	ME-XU8-5EV-1I-D12E	ME-XU8-7EV-1E-D11E	ME-XU8-7EV-2I-D12E

*** Notes**

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Valid as of October 5th 2021. Consult the product web pages for a full listing of available models.	Mercury+™ XU9			Mercury+™ XU6					
FPGA Family	Zynq® UltraScale+™			Zynq® UltraScale+™					
FPGA Device Name	ZU4CG	ZU5EV	ZU7EV	ZU2CG	ZU2EG	ZU3EG	ZU4CG	ZU4EV	ZU5EV
FPGA Speed Grade*2	1	1	2	1	1	2	1	1	2
FPGA Part Number*2	XCZU4CG-1FBVB900E	XCZU5EV-1FBVB900I	XCZU7EV-2FBVB900I	XCZU2CG-1SFVC784E	XCZU2EG-1SFVC784I	XCZU3EG-2SFVC784I	XCZU4CG-1SFVC784E	XCZU4EV-1SFVC784I	XCZU5EV-2SFVC784I
CPU Cores	2 x A53 | 2 x R5	4 x ARM® Cortex™-A53 | 2 x Cortex™-R5		2 x A53 | 2 x R5	4 x ARM® Cortex™-A53 | 2 x Cortex™-R5		2 x A53 | 2 x R5	4 x ARM® Cortex™-A53 | 2 x Cortex™-R5	
CPU Frequency @ MHz	1,200 | 500		1,333 | 533	1,200 | 500		1,333 | 533	1,200 | 500		1,333 | 533
PS Peripherals	DP | PCIe® Gen2 x4 SATA | SGMII | CAN	Mali™ | DisplayPort | PCIe® Gen2 x4 SATA | SGMII | CAN		DP | PCIe® Gen2 x4 SATA | SGMII | CAN	Mali™ | DisplayPort | PCIe® Gen2 x4 SATA | SGMII | CAN		DP | PCIe® Gen2 x4 SATA | SGMII | CAN	Mali™ | DisplayPort | PCIe® Gen2 x4 SATA | SGMII | CAN	
PS Ethernet | USB	2 x 1 Gbps | 2 x USB 3.0			1 Gbps | USB 3.0					
PS SDRAM Size (MByte)	2,048 + ECC	4,096 + ECC		1024	8,192 + ECC	2048	4096		4,096 + ECC
PS SDRAM Type | Bandwidth (MByte/s)	DDR4 | 19,200			DDR4 | 9,600	DDR4 | 19,200				
PL System Logic Cells	192'150	256'200	504'000	103'320		154'350	192'150		256'200
PL Block RAM (kbit)	18'432	23'616	38'880	5'400		7'776	18'432		23'616
PL DSP Systolic FIR (GMAC/s)	939	1'610	2'678	310		558	939		1'934
PL MGT Transceivers @ Gbps*6	16 @ 12.5		16 @ 15	-			4 @ 12.5		
PL Peripherals	PCIe® Gen3 x16	PCIe® Gen3 x16 | H.265 Codec		-			PCIe® Gen3 x4	PCIe® Gen3 x4 | H.265 Codec	
PL Ethernet | USB*5	-			-					
PL SDRAM Size (MByte)	2'048			-					
PL SDRAM Type | Bandwidth (MByte/s)	DDR4 | 19,200			-					
Flash Memory	64M QSPI | 16G eMMC			64M QSPI | 16G eMMC					
Connector Pins | IO Pins	504 | 192			504 | 274			504 | 294		
PL 3.3V | PL 1.8V | PL 1.2V Pins | PS Pins	52 | - | 26 | 14			96 | 144 | - | 14					
Module Dimensions (mm)	74 x 54			65 x 54					
Temperature Range*2	0..+85°C	-40..+85°C		0..+85°C	-40..+85°C		0..+85°C	-40..+85°C	
Boot Modes	QSPI | SD Card | eMMC			QSPI | SD Card | eMMC					
Product Status	Active			Active					
Estimated Product Lifetime*3	2030+			2030+					
Preferred Model | MOQ*4	No | 30	No | 20	Yes	Yes	Yes	No | 40	Yes	No | 40	Yes
Product Model	ME-XU9-4CG-1E-D11E	ME-XU9-5EV-1I-D12E-L11	ME-XU9-7EV-2I-D12E-L11	ME-XU6-2CG-1E-D10H	ME-XU6-2EG-1I-D13E	ME-XU6-3EG-2I-D11	ME-XU6-4CG-1E-D12	ME-XU6-4EV-1I-D12	ME-XU6-5EV-2I-D12E

*** Notes**

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Valid as of October 5th 2021. Consult the product web pages for a full listing of available models.	**Andromeda™ XZU90**		**Andromeda™ XZU65**		
FPGA Family	Zynq® UltraScale+™		Zynq® UltraScale+™		
FPGA Device Name	ZU17EG	ZU19EG	ZU7EG	ZU7EV	ZU11EG
FPGA Speed Grade*2	1	2	2	2	2
FPGA Part Number*2	XCZU17EG-FFVD1760E	XCZU19EG-2FFVD1760I	XCZU7EG-2FFVC1156I	XCZU7EV-2FFVC1156I	XCZU11EG-2FFVC1156I
CPU Cores	4 x ARM® Cortex™-A53 | 2 x Cortex™-R5		4 x ARM® Cortex™-A53 | 2 x Cortex™-R5		
CPU Frequency @ MHz	1,200 | 500	1,333 | 533	1,333 | 533		
PS Peripherals	Mali™ | DisplayPort | PCIe® Gen2 x4 SATA | SGMII | CAN		"Mali™ | DisplayPort | PCIe® Gen2 x4 SATA | SGMII | CAN"		
PS Ethernet | USB	1 Gbps | 1 x USB 3.0		1 Gbps | 1 x USB 3.0		
PS SDRAM Size (MByte)	4,096 + ECC	8,192 + ECC	4,096 + ECC		
PS SDRAM Type | Bandwidth (MByte/s)	DDR4 | 19,200		DDR4 | 19,200		
PL System Logic Cells	926'194	1'143'450	504'000	504'001	653'100
PL Block RAM (kbit)	58'032	72'288	38'880	38'880	44'640
PL DSP Systolic FIR (GMAC/s)	2'051	3'050	2'678	2'678	4'538
PL MGT Transceivers @ Gbps*6	28 @ 25 + 44 @ 12.5	28 @ 25 + 44 @ 16.3	20 @ 25		
PL Peripherals	4 x PCIe® Gen3 x16 2 x 150G Interlaken 2 x 100G Ethernet	5 x PCIe® Gen3 x16 4 x 150G Interlaken 4 x 100G Ethernet	PCIe® Gen3 x16	PCIe® Gen3 x16 | H.265 Codec	PCIe® Gen3 x16
PL Ethernet | USB*5	1 Gbps		1 Gbps		
PL SDRAM Size (MByte)	-		4'096		
PL SDRAM Type | Bandwidth (MByte/s)	-		DDR4 | 19,200		
Flash Memory	128M QSPI | 16G eMMC		128M QSPI | 16G eMMC		
Connector Pins | IO Pins	1440 | 686		720 | 322		
PL 3.3V | PL 1.8V | PL 1.2V Pins | PS Pins	24 | 260 | - | 22		24 | 156 | - | 22		
Module Dimensions (mm)	84 x 60		68 x 52		
Temperature Range*2	0..+85°C	-40..+85°C	-40..+85°C		
Boot Modes	QSPI | SD Card | eMMC		QSPI | SD Card | eMMC		
Product Status	Early Access		Development		
Estimated Product Lifetime*3	2030+		2030+		
Preferred Model | MOQ*4	TBD		TBD		
Product Model	AM-XZU90-17EG-1E-D12E	AM-XZU90-19EG-2I-D13E	AM-XZU65-7EG-2I-D3	AM-XZU65-7EV-2I-D3	AM-XZU65-11EG-2I-D3

*** Notes**
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Valid as of October 5th 2021. Consult the product web pages for a full listing of available models.	**Mars™ MA3**	**Mercury™ SA1**	**Mercury+™ SA2**	**Mercury+™ AA1**		
FPGA Family	Cyclone® V SX	Cyclone® V SX	Cyclone® V ST	Arria® 10		
FPGA Device Name	C6	C6	D6	SX 270	SX 270	SX 480
FPGA Speed Grade*2	7	7	7	3	2	2
FPGA Part Number*2	"5CSXFC6C6 U23I7N"	"5CSXFC6C6 U23I7N"	"5CSTFD6D5 F31I7N"	10AS027E4 F29E3SG	10AS027E2 F29I2SG	10AS048E3 F29I2SG
CPU Cores	2 x ARM® Cortex™-A9	2 x ARM® Cortex™-A9	2 x ARM® Cortex™-A9	2 x ARM® Cortex™-A9		
CPU Frequency @ MHz	800	800	800	1'000	1'200	1'200
HPS Cores & Peripherals	2 x CAN	2 x CAN	2 x CAN	3 x EMAC		
HPS Ethernet | USB	1 Gbps | USB 2.0 OTG	1 Gbps | USB 2.0 OTG	1 Gbps | USB 2.0	1 Gbps | USB 2.0		
HPS SDRAM Size (MByte)	1,024	1,024	2,048	2,048 + ECC		4,096 + ECC
HPS SDRAM Type | Bandwidth (MByte/s)	DDR3L | 3,200	DDR3L | 3,200	DDR3L | 3,200	DDR4 | 7,464	DDR4 | 8,532	DDR4 | 8,532
FPGA System Logic Elements	110'000	110'000	110'000	270'000		480'000
FPGA Block RAM (kbit)	5'570	5'570	5'570	15'000		28'620
FPGA DSP Systolic FIR (GMAC/s)	112	112	112	1'228	1'461	2'408
FPGA MGT Transceivers @ Gbps*6	2 @ 3.125	6 @ 3.125	9 @ 6.144	12 @ 10.3125	12 @ 12.5	
FPGA Peripherals	PCIe® Gen1 x2	PCIe® Gen1 x4	PCIe® Gen2 x4	PCIe® Gen3 x8		
FPGA Ethernet | USB*5	1 Gbps | 100 Mbps	-	2 x 100 Mbps | Cypress FX3™ USB 3.0	Cypress FX3™ USB 3.0		
FPGA SDRAM Size (MByte)	-	-	-	2,048 + ECC		4,096 + ECC
FPGA SDRAM Type | Bandwidth (MByte/s)	-	-	-	DDR4 | 7,464	DDR4 | 8,532	DDR4 | 8,532
Flash Memory	64M QSPI | 16G eMMC	64M QSPI | 16G eMMC	64M QSPI | 16G eMMC	64M QSPI | 16G eMMC		
Connector Pins | IO Pins	200 | 104	336 | 178	504 | 294	504 | 286		
FPGA 3.3V | FPGA 1.8V Pins | HPS Pins	76 | - | 16	134 | - | 16	234 | - | 18	- | 212 | 18		
Module Dimensions (mm)	67.6 x 30	56 x 54	74 x 54	74 x 54		
Temperature Range*2	-40..+85°C	-40..+85°C	-40..+85°C	0..+85°C	-40..+85°C	-40..+85°C
Boot Modes	QSPI | SD Card | eMMC	QSPI | SD Card | eMMC	QSPI | SD Card | USB3	QSPI | SD Card | eMMC | USB3		
Product Status	Active	Active	Active	Active		
Estimated Product Lifetime*3	2030+	2030+	2030+	2030+		
Preferred Model | MOQ*4	Yes	Yes	Yes	Yes	No | 40	Yes
Product Model	MA-MA3-C6-7I-D10	ME-SA1-C6-7I-D10	ME-SA2-D6-7I-D11	ME-AA1-270-3E4-D11E	ME-AA1-270-2I2-D11E	ME-AA1-480-2I3-D12E

*** Notes**
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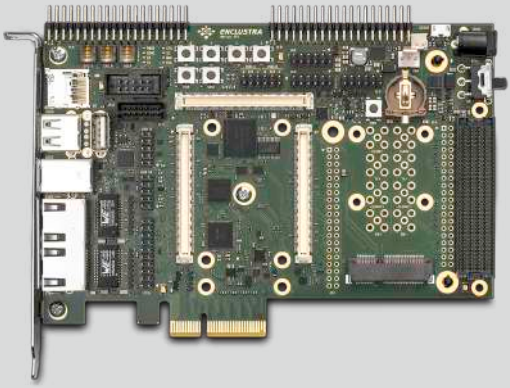
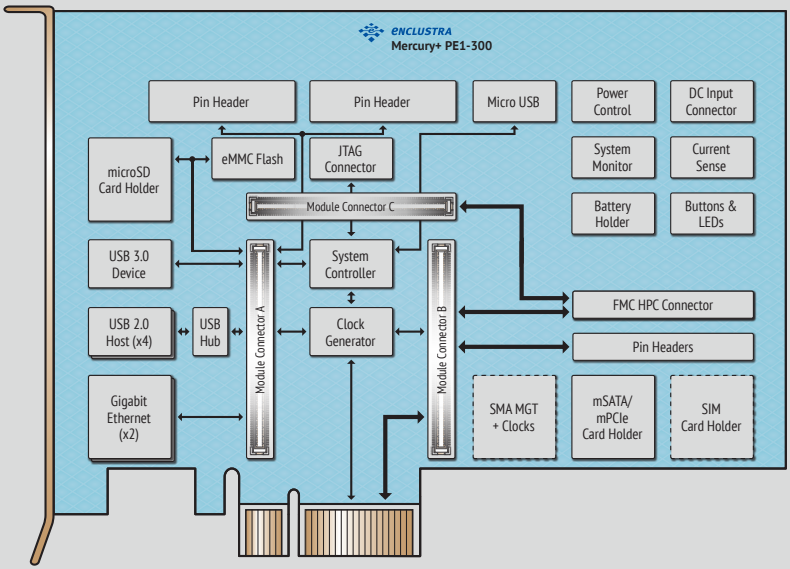
MERCURY+ PE1

PCIe® Base Board

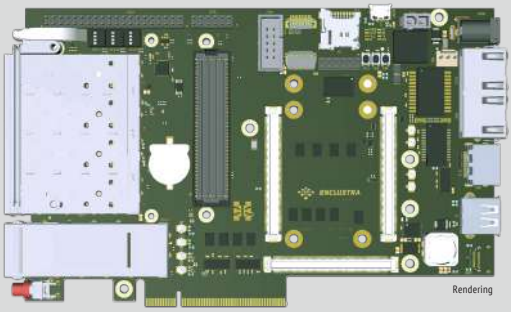


- Mercury module connectors
- Low-jitter clock generator
- PCIe × 4 interface
- USB 3.0 device
- Up to 4 × USB 2.0 host
- FTDI USB 2.0 High-speed device controller
- 2 × Gigabit Ethernet
- Up to 2 × FMC LPC/HPC connectors
- mPCIe/mSATA card holder
- microSD card holder
- 12 V single supply
- 160 × 111.2 mm (PCB only)
- Standalone or PCIe operation
- Available in three configurations (PE1-200/300/400)

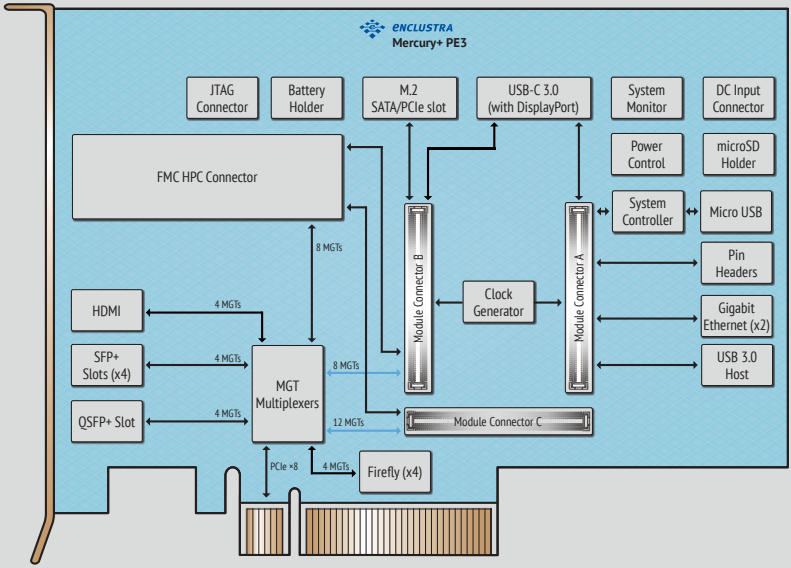


MERCURY+ PE3

PCIe® Base Board



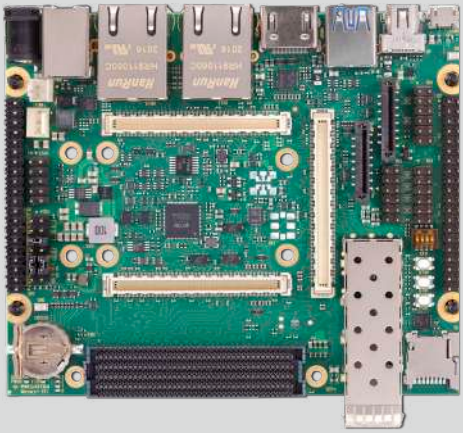
- Mercury module connectors
- PCIe × 8 interface
- QSFP+ slot, 4 × SFP+ slots
- USB 3.0 host connector
- USB-C 3.0 interface with DisplayPort support
- Samtec FireFly™ connector
- M.2 SATA/PCIe socket
- 2 × Gigabit Ethernet
- HDMI connector
- FMC HPC connector
- Low-jitter clock generator
- microSD card holder
- FTDI USB 2.0 High-Speed device controller
- System controller with USB JTAG/UART
- Standalone or PCIe operation
- 12 V single supply or USB-C powered
- 171 × 112.4 mm (PCB only)



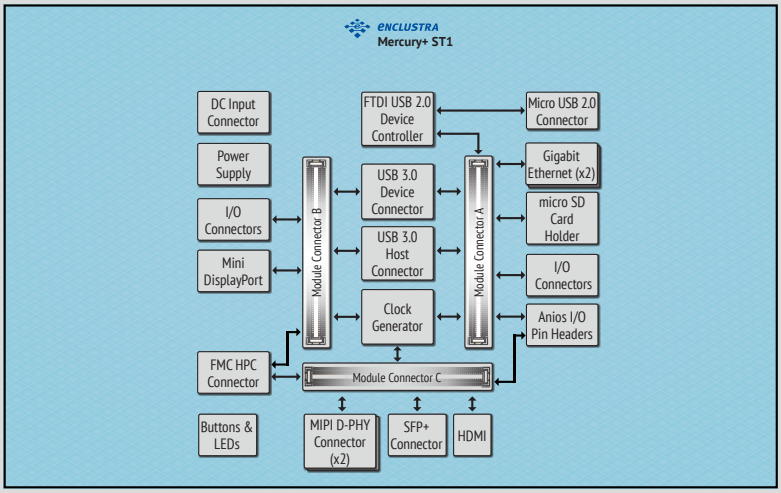
In development – please contact us for availability.

MERCURY+ ST1

Mercury Base Board



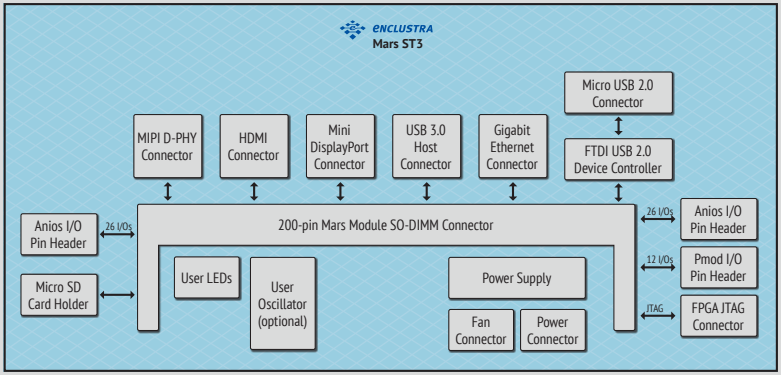
- Mercury module connectors
- USB 3.0 host connector
- USB 3.0 device connector
- FTDI USB 2.0 High-Speed device controller
- 2 × MIPI D-PHY interfaces (CSI and DSI/CSI)
- 2 × Gigabit Ethernet
- HDMI connector
- Mini DisplayPort connector
- SFP+ connector
- FMC HPC connector
- Low-jitter clock generator
- microSD card holder
- 2 × 40-pin Anios headers
- 3 × 12-pin I/O connectors
- 12 V single supply
- 100 × 120 mm



MARS ST3

Mars Base Board

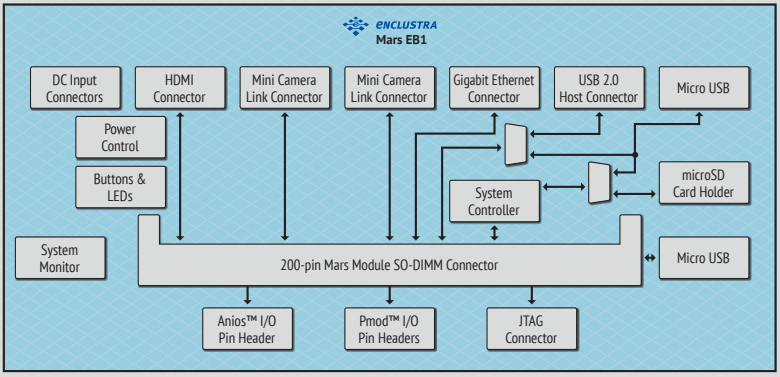
- Mars module connector
- FTDI USB 2.0 High-Speed device controller
- USB 3.0 host connector
- HDMI connector
- Mini DisplayPort connector
- MIPI D-PHY connector (CSI)
- Gigabit Ethernet
- 2 × 40-pin Anios headers
- Pmod I/O headers
- microSD card slot
- 12 V single supply
- 80 × 100 mm



MARS EB1

Mars Base Board

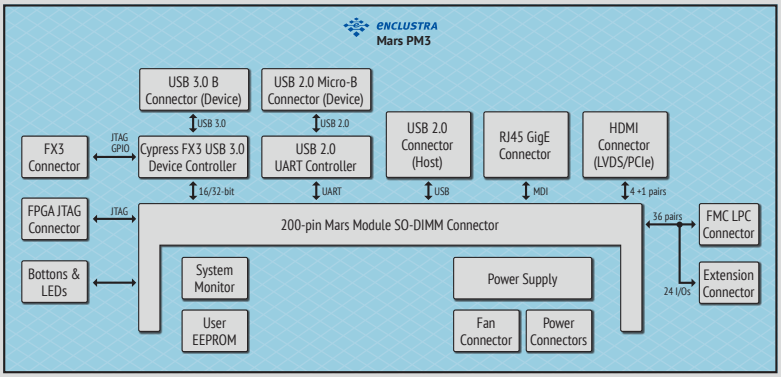
- Mars module connector
- FTDI USB 2.0 High-Speed device
- 2 × Mini Camera Link
- HDMI 1.3 connector
- Micro USB 2.0 device
- microSD card slot
- 42 user I/O pins
- 40-pin Anios headers
- 2 user buttons, 1 user LED
- 12 V single supply
- 120 × 80 mm



MARS PM3

Mars Base Board

- Mars module connector
- FMC LPC connector
- Mini HDMI connector
- Cypress FX3 USB 3.0 device controller
- USB 2.0 UART
- Gigabit Ethernet
- microSD card holder
- 12 V single supply
- p-ITX format (100 × 72 mm)



Linux Build Environment

A huge logo, for a tool that saves a huge amount of time.
Our Linux Build Environment is a free tool which users can use to build their own Linux for Enclustra modules – at the push of a button.

Select a target module and base board, let the tool do its thing, and all required binaries, such as the FPGA bitstream and boot loader, will be downloaded. It also downloads and compiles software such as U-Boot, Linux, and the BusyBox based root file system.

PetaLinux Board Support Packages (BSP) are provided for all Xilinx-based SoC modules to accelerate your development productivity.

Find more information on GitHub

Reference Designs, PetaLinux BSPs and Application Notes:

github.com/enclustra

Enclustra Build Environment (EBE):

github.com/enclustra-bsp

» Module Configuration Toolkit

An application

The Module Configuration Tool (MCT) is a free application which allows the user to configure our modules and base boards via USB, without additional hardware. No break-out boxes, no funky connectors – all you need is a USB cable.

A library

The library used by the MCT, MctLib, is also available free of charge in binary form; it allows users to integrate module enumeration, FPGA and SPI flash configuration, and I2C communication functionality in their own applications.

MctLib is available for both Windows and Linux, and consists of a flexible library with a C-style interface, allowing use of the library from almost any programming language. For C++ applications, a C++ wrapper is also provided for ease of use.

A flexible codebase

If you'd like to integrate or customize the Module Configuration Tool to your needs, we also offer a source code license for both the GUI and the MctLib library. Contact us for more information.

» Design Resources

In order to make integrating our products to customer designs as easy as possible, we provide a number of design support files to make the process as painless as possible.

3D Models

For all of our modules and base boards, 3D models are available to aid in the design of compatible custom hardware and enclosures.

User Manuals

Everything you always wanted to know about a module, but were afraid to ask: an A-Z of a module's hardware, features, and configuration options.

User Schematics

How the components on our hardware talk to each other.

Reference designs and Application Notes

Our reference designs are lovingly created to get your design off the ground quickly, in both HDL and software. Altium Design Files (Selected Base Boards)

Master Pinouts

Check the pinout of a module or base board, and compare it with other pin-compatible modules, even future modules that haven't been released yet.

Net Length Tables

High-speed design is tricky; net length tables give you exactly what you need to best plan for signal routing and integrity.

Online Support

For anything that isn't covered in the information above, our support staff are always on hand to help, even before purchase.

Linux Board Support Packages

Linux Board Support Packages (BSP) are provided for all SoC modules to accelerate your development productivity.

» Our IP Solutions

Accelerate your development

An IP Core from Enclustra will significantly reduce time to market as well as the total cost of ownership. We offer a range of flexible IP solutions, covering different application areas; here are a couple of things worth knowing:

They're royalty free

After you purchase an IP license, that's it; no recurring fees, no royalties, nada. The IP can be used perpetually, according to the license terms.

We offer different license models

The license itself can also be tailored to your requirements. We offer binary (encrypted VHDL) and source code licenses. For more information about licensing please visit enclustra.com/faq

Free evaluation

You can evaluate our IP solutions, with full functionality, before committing to buy. Just download the evaluation version on our web page.

We keep you up to date

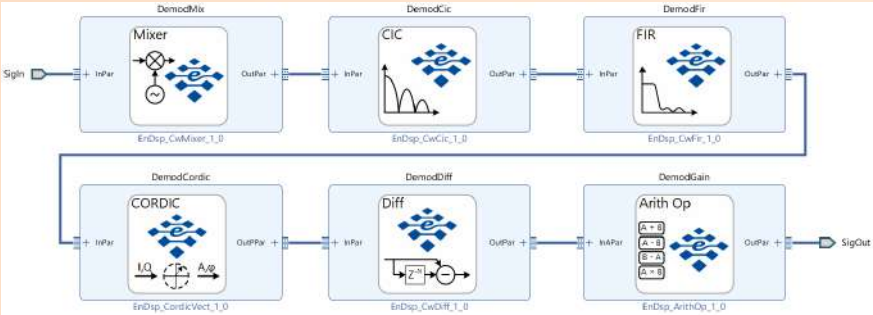
We offer maintenance agreements for our IP solutions to keep you provided with updates, enhancements and new device support. Maintenance for the first year is included in the license fee.

UNIVERSAL DSP LIBRARY

IP Solution

Create complex DSP systems in minutes

Enclustra's Universal DSP Library provides efficient FPGA implementations of the most common digital signal processing components, such as FIR and CIC filters, mixers, CORDIC and function approximations. It also provides the necessary glue logic needed to connect DSP systems together, such as multiplexers, stream splitters, buffers, TDM-parallel converters and fixed-point format converters.



Features

- Supports multiple independent data channels (both in parallel and TDM)
- Supports continuous wave (CW) and pulse processing
- Supports real and complex (IQ) signals
- Uses a standardized and simple interface specification, based on the widely-used AXI4-Stream protocol

Highlights

- Minimized development time
- Build signal processing chains rapidly using Vivado's Block Design GUI
- Every component is provided in both raw VHDL and a Xilinx Vivado IPI block
- Bit-true software models are provided for every DSP block (in Python), so the whole processing chain can be evaluated in software before stepping into FPGA implementation
- Reference designs are provided, showing how the IP blocks can be connected to form signal processing systems
- Full documentation and bit-true software models are available for free

Evaluation

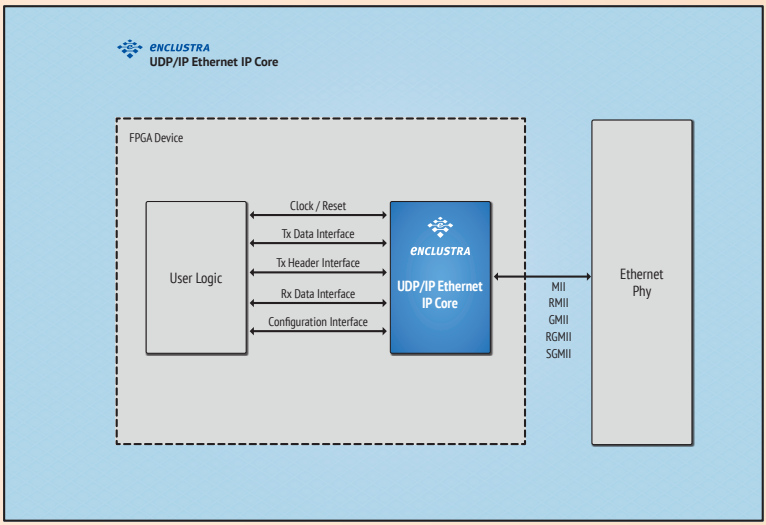
- A free IP evaluation license including reference design is available

UDP/IP ETHERNET

IP Core

Simple Ethernet communication, without a CPU.

The UDP/IP/Ethernet IP Core implements a versatile communication solution that allows data transfer via Ethernet using the UDP protocol without the need of a CPU or Ethernet stack. It provides easy to use FIFO/AXI-Stream interfaces on the FPGA side and connects to any Ethernet PHY. Optionally, non-UDP communication is supported for management and configuration as well. The IP core is able to operate at full 1 Gbit/sec wire speed. 100 Mbit/sec and 10 Mbit/sec operation is also supported.



Features and benefits

- No CPU or UDP stack needed
- Operates at full 1 GBit/sec wire speed
- Complete UDP, IPv4 and Ethernet layer processing
- Automatic ARP reply generation
- 1 Gbit/sec, 100 Mbit/sec and 10 Mbit/sec operation
- MII, RMII, GMII, RGMII and SGMII media independent interfaces (full-duplex only)
- Destination UDP port, destination IP address and destination MAC address filtering
- UDP checksum calculation and check
- Optional receive data buffers
- Multiple UDP ports with dedicated receive and transmit interfaces for each port
- Raw Ethernet port for non-UDP communication
- **Vendor independent:** Full integration with Intel® and Xilinx® tools

Evaluation

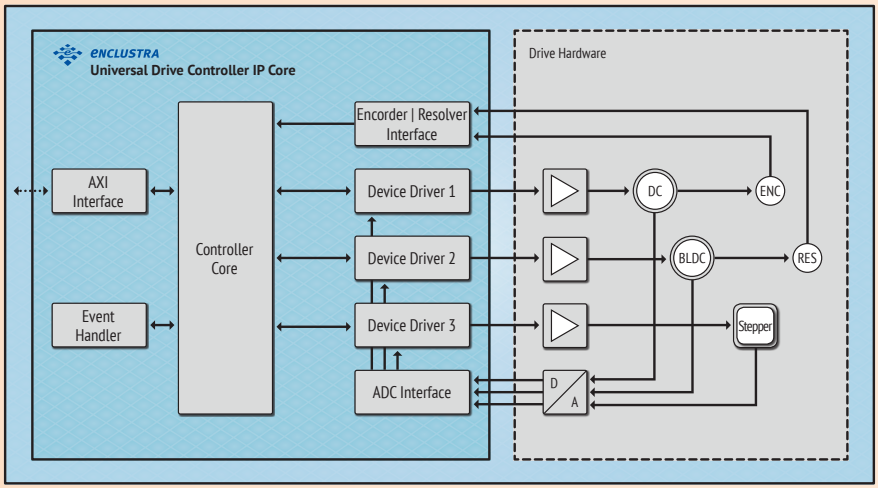
- Free evaluation version available
- Quick Start Kit, including support, is available

UNIVERSAL DRIVE CONTROLLER

IP Solution

High-performance FPGA/SoC motion control – supporting DC, BLDC and stepper motors

A highly optimized IP solution, featuring implementations of commonly-used motor control algorithms for position, velocity and current control, as well as all required interfaces to the power electronics. A simple and portable C programming API allows easy access to all features from software.



Features and benefits

- Control up to 8 motors simultaneously
- Control loop update rates of up to 200 kHz
- Fully autonomous event handling
- Supports BLDC, DC and stepper motors
- Features field-oriented control for BLDC motors
- Position control and trajectory planner
- **Vendor independent:** Full integration with Intel® and Xilinx® tools

Flexibility is key

- Full support for custom current, position and velocity measurement circuits
- Specify which controls loops are autonomous and which are implemented in software

Integration and ease of use

- C programming API to access all features
- Full integration with Intel® and Xilinx® tools
- Reference designs available for all motor types

Evaluation

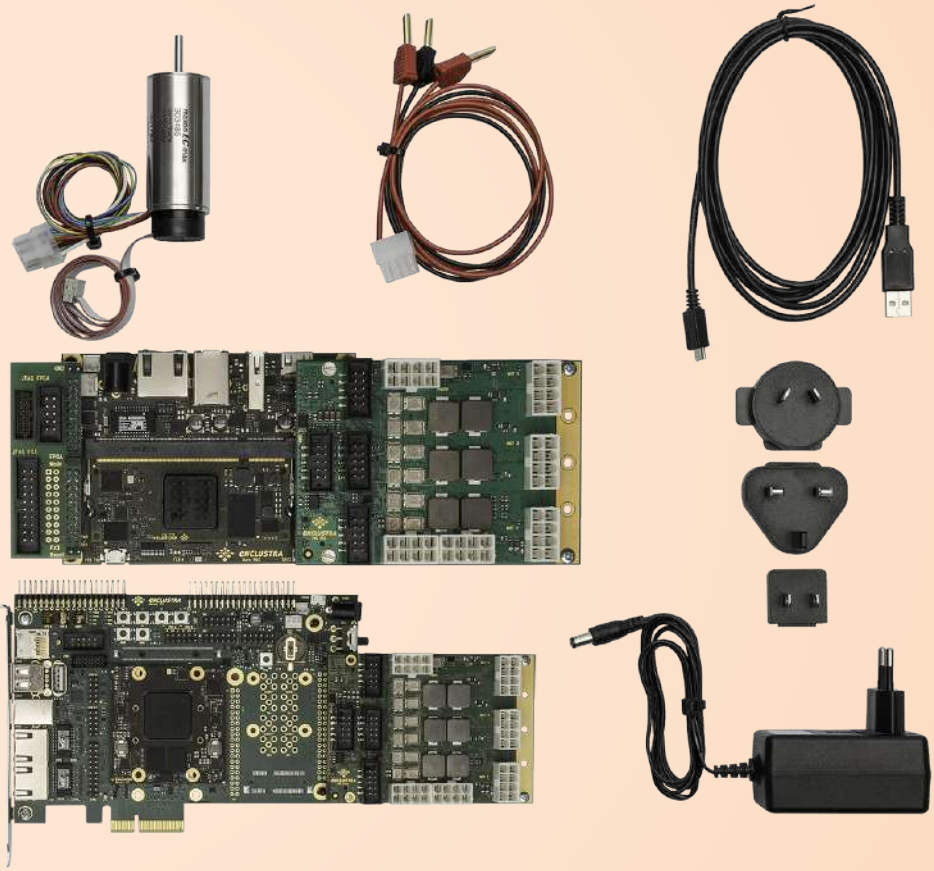
- A free IP evaluation license including reference design and example application is available
- Start with a spinning motor using a quick-start kit including an SoC module, base board, power electronics and motor. For more information see next page.

UNIVERSAL DRIVE CONTROLLER

Evaluation Kit

Get started with the Universal Drive Controller, right out of the box.

The Universal Drive Controller Evaluation Kit provides an out-of-the box hardware platform with reference design to both speed your development time and enhance your productivity.



The kit contains:

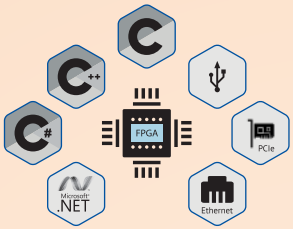
- Universal Drive Controller Evaluation License, with support for up to 2 DC, BLDC or stepper motors
- Intel: Mercury SA1 SoC module & Mercury+ PE1-200 base board
- Xilinx: Mars ZX3 SoC module & Mars PM3 base board
- FMC-DR2 drive control card
- BLDC (Maxon), DC or stepper motor
- Reference design
- 2 hours of support

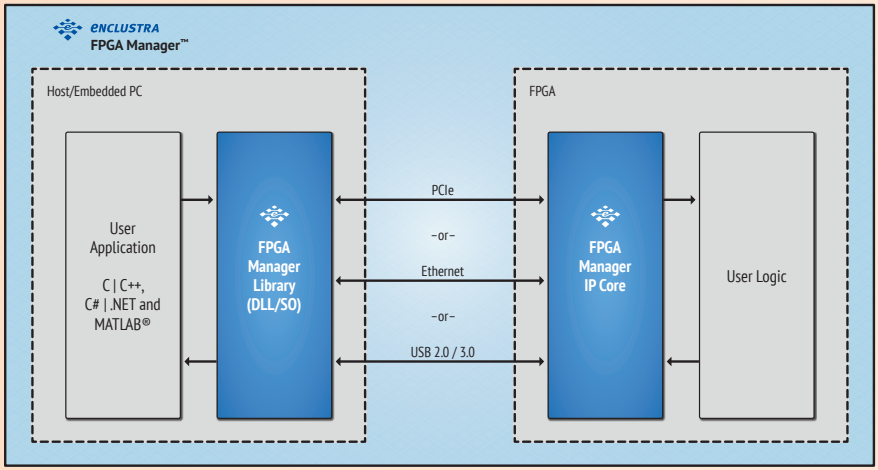
FPGA MANAGER

IP Solution

The clever solution to transfer data between FPGA and PC.

Transparently stream up to 16 data streams from FPGA to host, and vice versa, without needing to know the underlying protocols. PCIe® (Gen1-3, ×1-×8), USB 2.0, USB 3.0, and 10/100/1000 Mbps Ethernet links – all with one single API. Also supported are FPGA-in-the-loop applications, and memory-mapped access.





Software library

- Simple API with intuitive read/write functions
- C | C++ | C# .NET Core
- Supports Windows and Linux

FPGA IP core

- Supports standard bus interfaces
- Integrates into FPGA vendor tools for simple drag and drop instantiation
- Also available as a software implementation for PCs (FPGA modelling) or SoC FPGAs (co-processing)

Vendor independent

- Full integration with Intel® and Xilinx® tools

Base license

- PCIe, USB 3.0, USB 2.0 or Gigabit Ethernet
- 2 streams
- C | C++ and C# | .NET
- Windows or Linux

Evaluation

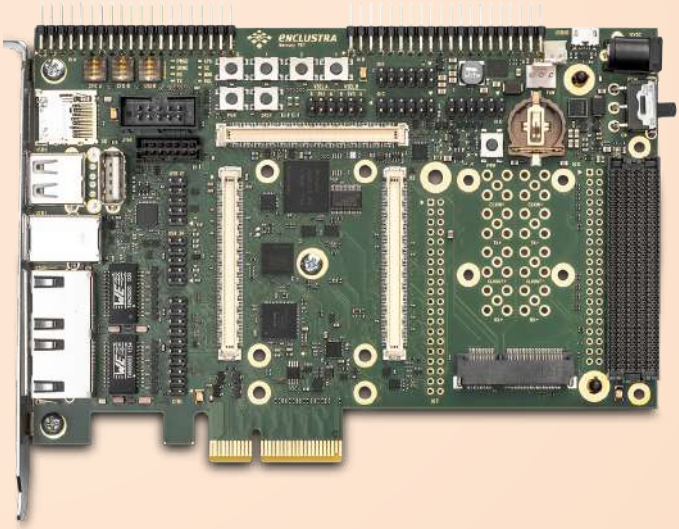
- Quick Start Kits, including support, are available
- Free evaluation version available

FPGA MANAGER

Evaluation Kit

Get started with the FPGA Manager, right out of the box.

The FPGA Manager™ Evaluation Kit provides a full featured design platform to build communication centric applications for PCIe®, Ethernet and USB 3.0. The kit provides an out-of-the box hardware platform with reference design to both speed your development time and enhance your productivity. It contains following components.



The kit contains:

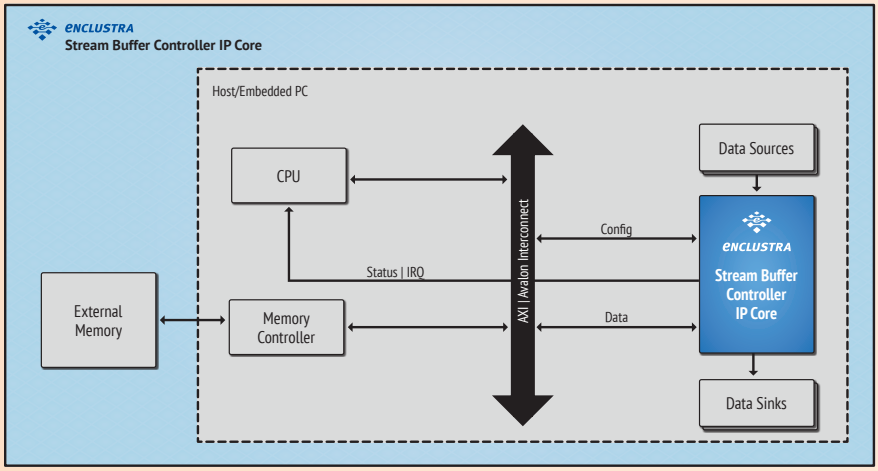
- FPGA Manager IP Solution, Evaluation License
- Reference design
- Mercury KX1 FPGA module
- Mercury+ PE1-200 base board
- Power supply
- 2 hours support included

STREAM BUFFER CONTROLLER

IP Core

Large, multi-stream FIFO handling.

A versatile IP core that implements a stream to memory mapped DMA bridge with up to 16 independent streams. The IP core allows data buffering in an external memory device to provide virtual FIFO capability, with up to 4 GB of memory. A simple C programming API is provided, as is the option to easily integrate with FPGA Manager™.



Features and benefits

- **Standalone solution:** A CPU can be easily replaced by a stream configuration controller that is provided in VHDL
- **Flexible data width conversion:** Conversion to/from any byte-multiple width for the write and read data streams
- **Highly configurable:** Operation mode, buffer size and buffer address can be set independently for each stream
- **Vendor independent:** Full integration with Intel® and Xilinx® tools

Evaluation

- **FIFO mode** Writes and reads are done over the AXI4-Stream interfaces
- **Write mode** Writes are done over the AXI4-Stream, reads are done by a CPU
- **Read mode** Writes are done by a CPU, reads are done over the AXI4-Stream interface
- **ROM mode** Reads are done over the AXI4-Stream interface (the memory must be initially written by a CPU)
- Free evaluation version available

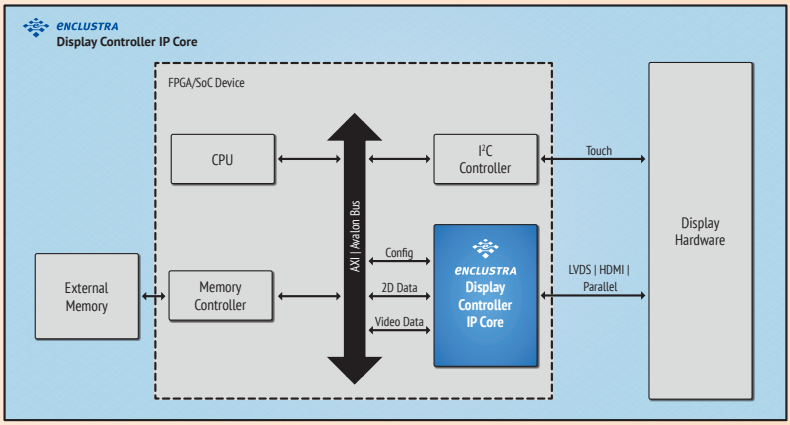
DISPLAY CONTROLLER

IP Core

Low-resource display control, with support for different display interfaces.

The Display Controller IP Core enables the easy addition of a display to existing or future FPGA designs, allowing the system designer to focus on the main application instead of dealing with display control issues. In addition, there is no need for an external display controller device that would consume precious PCB space and unnecessarily extend the project's BOM.

With its modular design and strong scalability, the Display Controller IP Core perfectly fits the system requirements without wasting any FPGA resources. These unique features will also simplify the reuse of the Display Controller IP Core in future projects. Selecting our Display Controller IP Core for the display control needs of present or future projects will significantly reduce time to market as well as the overall system cost.



Features and benefits

- Support for parallel, LVDS and HDMI/DVI displays without external display controller device
- Support for unlimited video pages
- Built-in PWM generator for display brightness control
- Optional 2D accelerator unit (draw/copy rectangles, supports transparent color)
- AXI bus interface for both register bank and frame buffer memory access
- Linux driver
- Support for AXI-Stream to interface with other IP Cores (e.g. HD-SDI transmitter)
- **Vendor independent:** Full integration with Intel® and Xilinx® tools

Evaluation

- Free evaluation version available

» Further Information

Pricing
Pricing is shown for specific module models and quantities – for a complete list of module models, and volume pricing for quantities of 1+, 30+, 100+, 300+, 1000+, 3000+ and 10000+, visit **www.enclustra.com**

Custom models
All hardware products can be tailored to specific applications in custom models (different FPGA part numbers, different memory sizes, etc.).

Custom hardware design
We often work together with customers to develop a brand new, application-specific hardware product. This can be a module, base board, or entire system; development costs and production rights may be shared, leaving both parties to benefit.

FAQ
More information and frequently asked questions can be found at www.enclustra.com/faq

Disclaimer
All prices are non-binding estimates – please contact us for definitive pricing and lead-time information. Information contained in this flyer is correct as of October 5th 2021, but is subject to change without notice. Trademarks used are property of their respective owners.

ENCLUSTRA
FPGA SOLUTIONS

Catalogue Autumn 2021

Development and Design Services

EVERYTHING FPGA.

About Enclustra

The company was founded in 2004 by Martin Heimlicher, with the aim of providing comprehensive FPGA solutions, from design through to production.

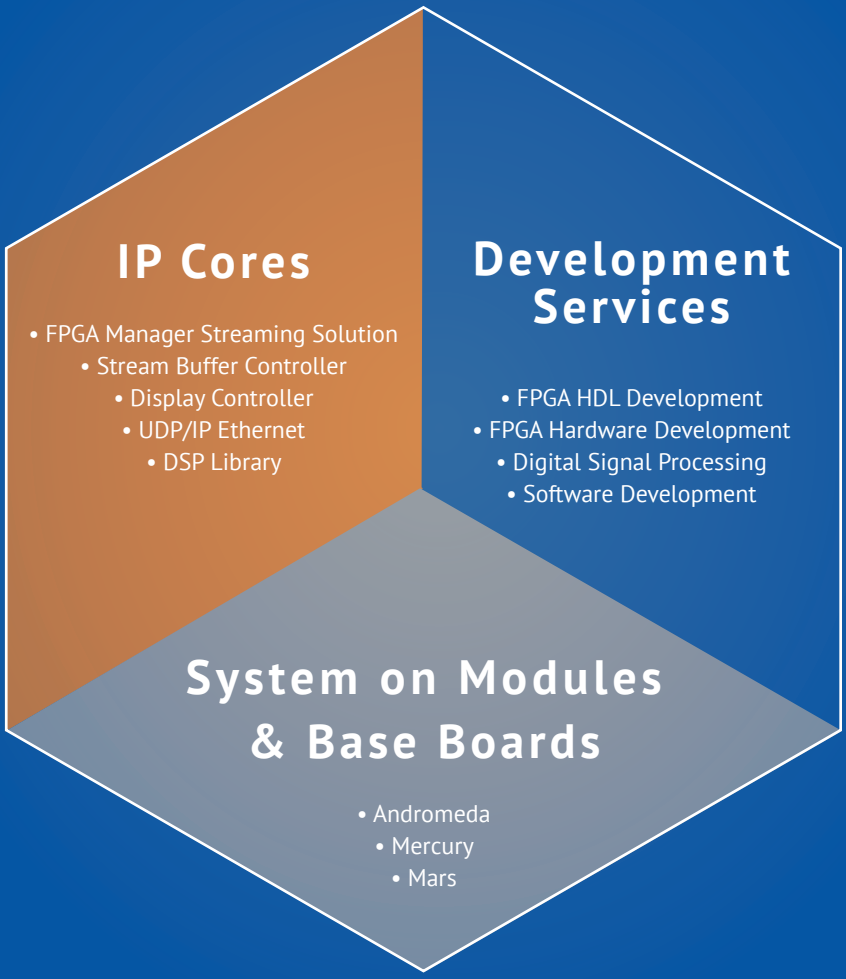
We currently have more than 60 people in our team, of 16 different nationalities, and we're growing.

Demand for our design services, FPGA modules and base boards is growing – our current customer base stands at over 1600 customers in over 70 countries, and continues to expand.

In addition to our main office, we have a subsidiary in China and sales and support offices in Germany, France, USA, Canada and the UK.

Our headquarters are located in the thriving Binz quarter in Zürich, Switzerland – an ideal location in one of the world's leading cities for technology and innovation.

» What we offer



We deploy leading edge technologies, and we're design service partners of Intel®, Xilinx® and Microchip® – this close collaboration allows us to be forward-looking in our design process, and remain on the cutting edge of the most advanced FPGA technology.

intel FPGA Design Solutions Network

XILINX Certified Partner

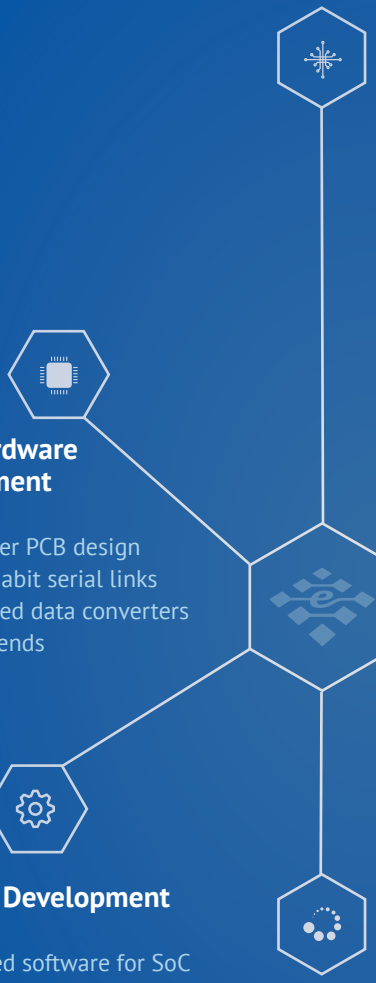
FPGA MICROCHIP DESIGN PARTNER

» Main Application Areas

We carry out customer projects in a wide array of application fields – below are some of the areas we're particularly experienced in.

- **Wired Networks and Switching (Ethernet)**
- **Industrial Communication (CAN)**
- **Wireless Communication (Software Defined Radio)**
- **Embedded Interfaces (PCIe, USB, AXI, etc.)**
- **Drive and Motion Control**
- **Computer Vision and Smart Cameras**
- **Test and Measurement / Data Acquisition**
- **Waveform Synthesis**

» Our Core Competencies



FPGA HDL Development

- Systems at the technical limits (complexity, bandwidth, processing power, latency)
- Integration of microcontrollers and peripherals
- Thorough verification and continuous integration
- HLS or HDL design entry

FPGA Hardware Development

- Multi-layer PCB design
- Multi-gigabit serial links
- High-speed data converters
- RF front ends

Video/Image Processing

- Smart cameras, frame grabbers
- Medical, broadcast, test and measurement, surveillance and security
- Custom algorithm implementation from Python, MATLAB, OpenCV, C/C++ or .NET/C# models

Software Development

- Embedded software for SoC and soft core processors
- Real-time control loops
- Linux BSPs and device drivers
- Host computer software as user interface to FPGA-based systems

Digital Signal Processing

- Bit-true Python/MATLAB/Simulink to VHDL conversion
- Resource-optimized implementation
- Software defined radio (channel filtering, sample rate conversion, modulation/demodulation, etc.)

» Digital Signal Processing

Manual, Bit-True HDL Implementation
Do you have a Python or MATLAB® implementation of a signal processing algorithm and need a best performance, lowest resource usage and lowest power FPGA implementation? Our engineering team has successfully completed a significant number of such projects with the help of our fixed-point arithmetics library.

Our fixed-point arithmetics library implements basic to medium-complexity fixed-point arithmetic functions in Python, MATLAB and VHDL. The implementations of the same function in Python, MATLAB and VHDL show exactly the same, bit-accurate behavior. The functions operate on the native data types of the individual languages and are thus easy to use.

The bit-true behavior is enabled by associating a fixed-point format to every operand and result. We take care of the algorithm's FPGA-optimization, and work with you to ensure that the FPGA-optimized Python or MATLAB algorithm still meets your requirements. After that, it's a straightforward path to a bit-true FPGA implementation, without any lengthy and costly iterations back through the algorithm design and optimization phases.

Universal DSP Library
For many FPGA designs, time to market is more important than lowest resource usage and lowest power, especially since newer FPGA generations provide more and more resources per cost and become more and more power-efficient. In such a scenario, manual HDL implementation may not be the best choice.

Enclustra's DSP library, which is based on Enclustra's fixed-point arithmetics library, provides ready-to-use Vivado IPI blocks that implement the most common DSP functionalities (filters, mixers, CORDIC, function approximations, etc.) and often underestimated glue logic (multiplexers, demultiplexers, buffers, TDM-to-parallel converters, etc.). The EN-DSP library enables simple and quick implementation and bit-true verification of the most common DSP functionalities. All blocks use a common interface convention (based on AXI4-Stream) and natively support parallel and TDM channels, continuous wave or pulse processing as well as real and complex signals.

Employing Enclustra's EN-DSP library in the context of a design service project allows for an optimum trade-off between development effort and resource efficiency.

Automated HDL Code Generation
If rapid prototyping and traceability are your main concerns, and target device cost is not in your focus in that phase, automated HDL code generation could be a useful option. Enclustra has successfully completed many projects employing tools like Xilinx Vitis/HLS and MathWorks HDL Coder to automatically generate HDL code from C/C++/MATLAB/Simulink sources.

An additional benefit of this approach is that application specialists – who not necessarily are FPGA experts – are able to develop the FPGA's signal processing units in their known environment and programming language, while Enclustra takes care of the communication infrastructure and interfaces.

Vision

Perspective Through Stereo

Introduction

What was once only possible in crime series is now a reality: 3D scans of forensic evidence found at crime scenes, recording minute details to be later analyzed from all angles. Enclustra developed the main elements of the 3D-Forensics scanner.

Customer Challenge

Procure an FPGA-based electronic system that is small enough to fit into the hand-held case, performant enough to meet the functional requirements and power-efficient enough to ensure a reasonable battery runtime.

The Solution

A system based on the Enclustra Mars AX3 module projects interference patterns through a miniaturized beamer attached via HDMI and simultaneously captures stereo images via two cameras connected to the Mars EB1 base board over Camera Link. The FPGA firmware running on the Mars AX3 then streams the data to a host PC via Enclustra's FPGA Manager Ethernet IP solution.

The Result

A compact, cost-effective FPGA-platform as the heart of the 3D-Forensics scanner solution.

Keywords
Xilinx® Artix™-7, Camera Link, Gigabit Ethernet, Xilinx MicroBlaze™, VHDL, C, C#, FPGA Hardware, FPGA Firmware, Embedded Software, Host Computer Software, Mars AX3, Mars EB1, FPGA Manager™ Ethernet

Space

FPGA to Satellite: Please Respond

Introduction

A reliable data connection between a satellite and the ground station is essential to the success of any satellite mission – to this end, one of our customers from space industry asked us to develop a data transmission testing system.

Customer Challenge

The testing system (special checkout equipment, SCOE) is used to verify the communication between individual satellite components as well as the communication between the satellite and the ground station. It needs to be able to transfer, record, store and check huge amounts of data, simulate the most extreme scenarios and provoke potential errors that can occur during the communication. The customer had difficulties finding such a specific solution off-the-shelf, so they opted for a contract development with Enclustra.

The Solution

In this project, our engineering team designed-in the Mercury KX1 module, mounted on a custom PCIe®-capable base board utilizing Enclustra's FPGA Manager™ PCI Express IP solution. The complete FPGA firmware that handles the employed protocols in real-time, as well as the host computer software, providing a GUI for setting up, running and analyzing the communication tests, were developed by our engineering team.

The Result

«Enclustra provided us with a turnkey development of a special checkout equipment (SCOE) for intra-satellite communication testing in the context of the SARah satellite mission. Their full-stack expertise, from PCB over FPGA firmware to application software development, made them a one-stop-shop for our needs. We will happily consider them again for our future projects.» Rafael Plonka, Team Lead, OHB System AG

Keywords
Xilinx® Kintex®-7, WizardLink, VHDL, C#, C++, FPGA System Design, FPGA Hardware, FPGA Firmware, Host Computer Software, Mercury KX1, FPGA Manager PCIe®, SCOE, Satellite

Aviation

Zynq UltraScale+ Drone Controller

Introduction

The official term is unmanned aerial vehicle (UAV), apparently, which is a bit of a mouthful, so we prefer to say drone. Drone tech evolved tremendously over the past decades. Nowadays, they can be used in construction, agriculture, photography, entertainment, and many other areas. In any case, we developed a flight and video controller for a UAV (drone) for a customer.

Customer Challenge

The customer required a hybrid FPGA/CPU hardware that is able to fulfill the performance and functional requirements while taking up as little room and weight in the vehicle as possible and, at the same time, is so power-efficient that a passive cooling solution would be sufficient. In addition, the hardware needs to be fit to reliably operate in harsh conditions (vibration and temperature).

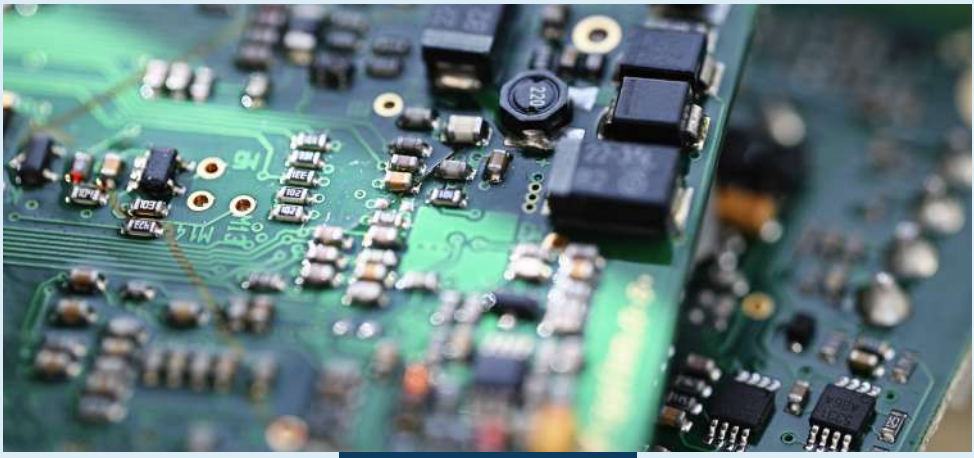
The Solution

Our engineering team employed a Xilinx Zynq UltraScale+ MPSoC, whose CPUs implement the position control as well as tracking of the flight trajectory. The sensors and actors are attached through the FPGA logic; the number and type of these interfaces vary greatly with the application of controlled vehicle, so all of these interfaces are dynamically configurable. The controller supports redundancy by having two parallel flight controller units supervising each other. Should the currently active flight controller fail, the reserve unit takes over all tasks autonomously. Aside flight control functions, the controller prepares and compresses a Full-HD video signal (HD-SDI) from a camera for transmission over radio.

The Result

A compact, powerful and very flexible flight and video controller. It is not only rugged but also very reliable thanks to the built-in redundancy.

Keywords
Xilinx® Zynq® UltraScale+®, Mentor Graphics PADS®, HD-SDI, VHDL, C, C++, FPGA System Design, FPGA Hardware, FPGA Firmware, Embedded Software



Communication

PCI Express to Wishbone Bridge

Introduction

We were asked to migrate the SPI slave interface of an existing FPGA design to PCIe® interface providing massively more bandwidth, while maintaining the FPGA-internal Wishbone communication infrastructure and as much as possible of the embedded software controlling the SPI master.

Customer Challenge

The main challenges for our customer were increasing performance requirements for the FPGA/CPU-interface and the lack of FPGA design expertise in their own development team. Also, the migration from SPI to PCIe should be transparent to the customer's already existing host software application.

The Solution

We replaced the SPI slave interface with a multi-function PCIe endpoint with attached Wishbone masters and mapped the new FPGA design to an Intel® Cyclone® V GX device. In addition to the Wishbone masters, a sophisticated DMA engine, which takes care of the higher-bandwidth data transfers, was developed. On the embedded software side, the low-level SPI driver was replaced by a tailored PCIe driver, providing the same API and emulating the same behavior.

The Result

«Enclustra reworked and extended our existing FPGA design, which is a central part of a series of specialized measurement devices. Enclustra represents the FPGA expertise in our development team, and we look forward to working with them to further extend the functionality of our product line.» Florian Leitner, Leiter Sondermaschinenbau Elektrotechnik, Schaeffler Technologies AG & Co. KG .

Keywords
Intel® Cyclone® V, PCI Express, Wishbone, DMA, VHDL, FPGA System Design, FPGA DHL, Embedded Software

Test & Measurement

Spectrum Analyzer

Introduction

Enclustra developed a Hand-held spectrum analyzer with real-time signal processing path. It includes elaborate filtering, down-conversion, Fourier-transform and analysis of important properties of the resulting signal. As an additional feature, signals can be demodulated in real-time.

Customer Challenge

Because the device runs from battery, it requires low power consumption while keeping the high performance and being compact at the same time.

The Solution

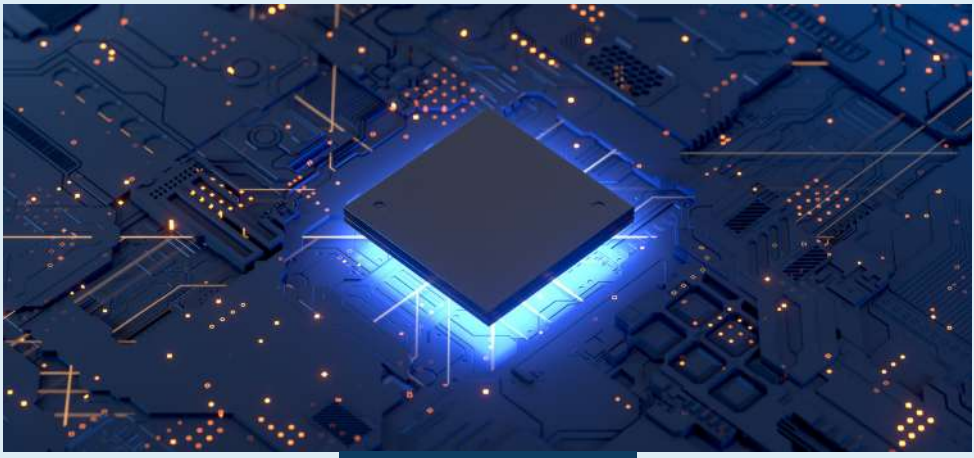
To meet the requirements, the complete signal processing path is realized in a low-cost, low-power Xilinx Artix-7 device. Thanks to Enclustra's approach of providing bit-true models first, the customer was able to evaluate the signal performance of the system even before HDL FPGA implementation was started.

Thanks to the modular VHDL code and the already existing unit and top-level regression tests, it was fairly simple to integrate the additional functionality and deliver a reliable system with stunning new features.

The Result

«One of the main parts in the digital signal processing path of Narda's Real-Time Spectrum Analyzer SignalShark has been developed and implemented by Enclustra. We appreciated Enclustra's professional approach, thorough documentation and deep understanding of signal processing algorithms as well as FPGA technology.» Eduard Staller, Director R&D, Narda Safety Test Solutions GmbH.

Keywords
Xilinx® Artix-7, DDR SDRAM, VHDL, MATLAB, Xilinx MicroBlaze, FPGA System Design, FPGA HDL, Embedded Software



Industrial

CPLD Replaces Discontinued IC

Introduction

What to do when a chip you're using is discontinued and you don't want to change your PCB layout? One of our customers came to us with this tricky question and asked us to develop a drop-in replacement for the discontinued keypad encoder IC.

Customer Challenge

The main challenge was to replace a no longer available IC with a drop-in replacement, so that no PCB layout, firmware or software changes were required to the rest of the system.

The Solution

Luckily, the chip housing was the «outdated» dual in-line (DIL) package – this allowed us to use a CPLD in a compact ball grid array package to reproduce the same functionality, and then assemble it to a PCB that reproduces the DIL form factor.

The Result

A small PCB accommodates the CPLD and DIL pin headers, and then slots seamlessly into the mainboard – without any PCB layout, firmware and software changes.

Keywords
Intel® MAX® V, VHDL, FPGA System Design, FPGA Hardware, FPGA HDL

AI / Machine Learning

Neural Network on SOM

Introduction

FPGA technology is becoming a major player in the field of embedded AI applications due to its ability to implement complex neural networks with low power consumption and low latency, while simultaneously interfacing a large number of peripherals and providing high levels of robustness, important for industrial applications.

Customer Challenge

In this case, Enclustra was their own customer. The challenge was to explore the potential of FPGAs in embedded AI applications and showcase it through a demo system.

The Solution

Based on the Mars XU3 module, featuring a Xilinx Zynq UltraScale+ MPSoC device, mounted on the Mars ST3 base board, the application employs popular neural networks like resnet50 and SSD for image classification and real-time face detection, respectively. The images are captured with a standard USB camera, connected to the Mars ST3 base board. For higher performance a MIPI interface can be used, also available on the Mars ST3. The live image with added overlays can then be viewed on a DisplayPort-capable monitor. Moreover, adding actuators such as BLDC or stepper motors is a straightforward task using Enclustra's Universal Drive Controller IP Core.

The Result

Enclustra successfully deployed an AI-powered embedded real-time image processing application to run on Enclustra's own SoC Module, which now serves as a demo system.

Keywords

Xilinx® Zynq® UltraScale+®, VHDL, Mentor Graphics ModelSim®, Xilinx DNNDK, C++, Linux, Mars XU3, Mars ST3, resnet50, SSD, USB, DisplayPort, MIPI

» Our Development Process

	Customer Enquiry
Requirements Engineering	Requirements definition | Use cases
Concept Engineering	Rough concept | Feasibility evaluation | Risk analysis Rough effort/cost estimation
Free Commercial Offer Creation	Project scope | Project schedule | Binding effort/cost estimation
	Purchase Order
Project Preparation	Project team setup | Project management setup | Kick-off
Detailed Hardware Design **Detailed HDL Design** **Detailed Software Design**	Detailed design of building blocks | Design documentation Peer reviews
Hardware Production **HDL Implementation System** **Software Implementation**	Implementation of building blocks | Block-level tests and simulation | Design documentation update | Peer reviews
Hardware Bringup & Test **HDL Integration & Test** **Software Integration & Test**	Integration of building blocks | Top-level tests and simulation Design documentation update | Peer reviews
System Integration & Test	System integration (HW, HDL and SW) | System-level tests Design documentation update
System Deployment	Release creation and delivery | Customer training Customer acceptance tests
	Customer Acceptance
System Maintenance	Maintenance | Support | Follow-up projects

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