



**Embedded Linux  
Conference**

Europe



**OpenIoT Summit**  
Europe

**Preempt-RT Latency  
Benchmarking of the  
Cortex-A53 processor**

**Paul Thomas, AMSC**  
**[Paul.thomas@amsc.com](mailto:Paul.thomas@amsc.com)**

# AMSC

- Founded in 1987
- Headquartered near Boston, Massachusetts
- Specializing in the design and manufacture of power systems and superconducting wire



# Preempt-RT Latency Benchmarking of the Cortex-A53

- Software and Hardware setup
- Basic Latency Tests
- UDP Ping Pong Ethernet Latency
- Real-World ADC Interrupt Latency

# Why Real-Time Linux?

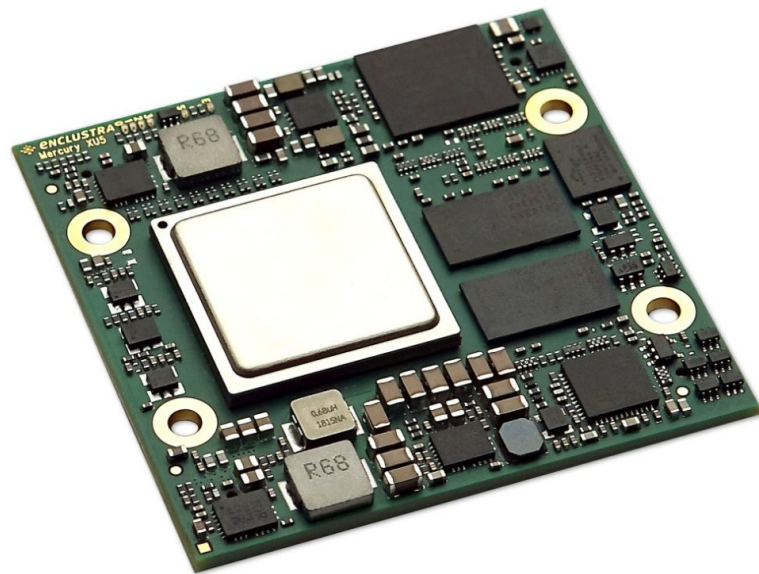
- Stable and supported code base
- Deep APIs (networking, fs, IPC, etc...)
- Good latency performance
- Real Time Linux collaborative project aims to mainline Preempt RT

# Processors and Boards that use the ARM Cortex-A53

- Xilinx Zynq UltraScale+ MPSoC
- NXP i.MX 8
- Raspberry PI 3
- ODroid-C2

# Hardware Setup

- ARM Cortex A53
  - Module: Enclustra Mercury XU5
  - SOC: Xilinx MPSoC XCZU5EV
  - 8 stage pipeline
  - 1.3 Ghz
- ARM Cortex A9
  - Board: Zedboard
  - SOC: Xilinx XC7Z020
  - 10+ stage pipeline
  - 666 MHz

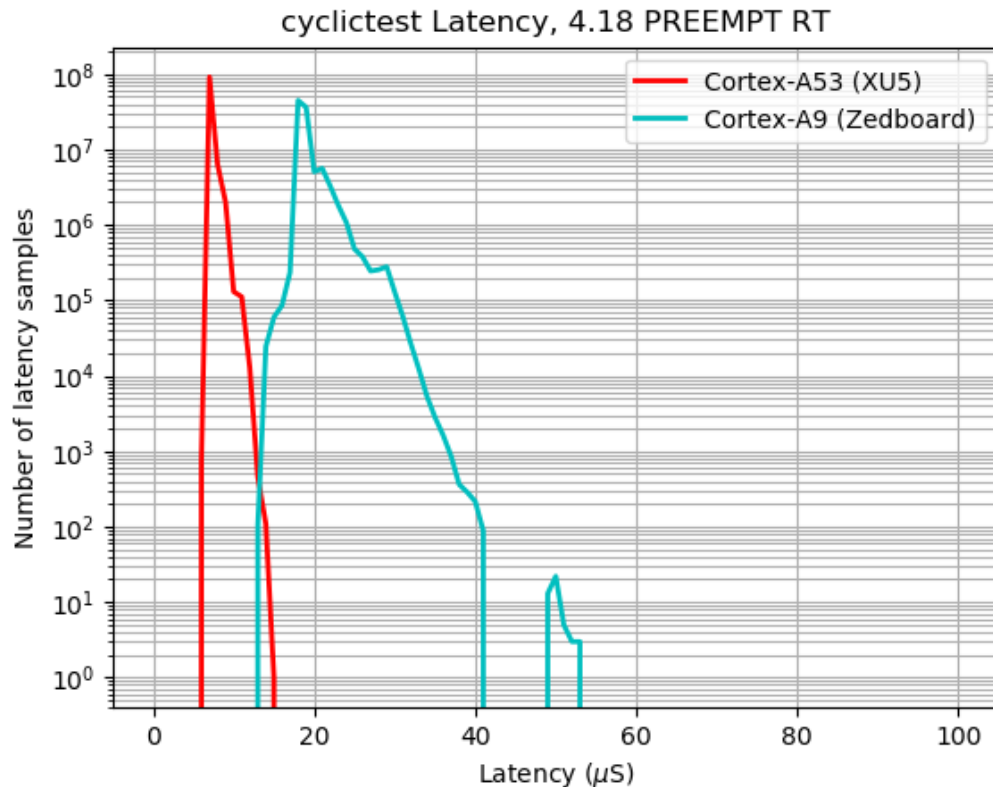


# Kernel

- Starting point is 4.18
- PREEMPT\_RT 4.18-rc8-rt1 patch applied
  - <https://cdn.kernel.org/pub/linux/kernel/projects/rt/4.18/older/patch-4.18-rc8-rt1.patch.xz>
- Zynqmp firmware and clock driver patch applied
  - <https://patchwork.kernel.org/project/linux-arm-kernel/list/?series=5175>

# Cyclictest Results

- Cortex-A53
  - Maximum: 17  $\mu\text{S}$
  - Mode: 7  $\mu\text{S}$
- Cortex-A9
  - Maximum: 54  $\mu\text{S}$
  - Mode: 19  $\mu\text{S}$





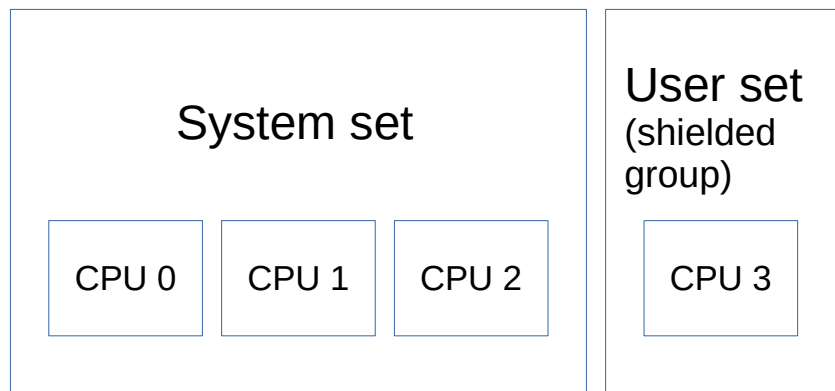
# Cpusets Shielding

- Kernel portion is CPUSSETS
- Userspace management via cpuset
  - <https://github.com/lpechacek/cpuset>

“Cpuset is a Python application that forms a wrapper around the standard Linux filesystem calls to make using the cpusets facilities in the Linux kernel easier”
- CPUSSETS is an effective way to shield 1 or more cores from scheduling ordinary tasks

# CPUSET and Loading Configuration

CPUSET Configuration<sub>1</sub>



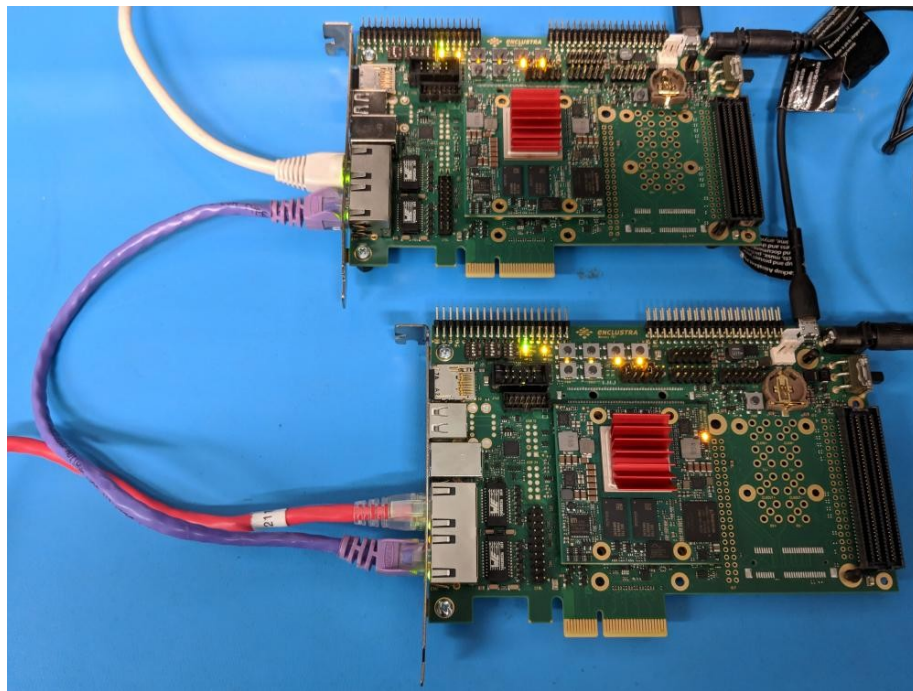
Cortex-A9 is only dual core,  
System set is just 1 core<sub>1</sub>

```
stress --cpu 8 --vm 8 --vm-bytes 20MB
```

- Test Configuration
  - System Set
    - Cyclicttest w/ priority 98
    - Cyclicttest w/ priority 99
    - Stress<sub>2</sub>
  - User Set
    - Cyclicttest w/ priority 98
    - Cyclicttest w/ priority 99 (results presented)

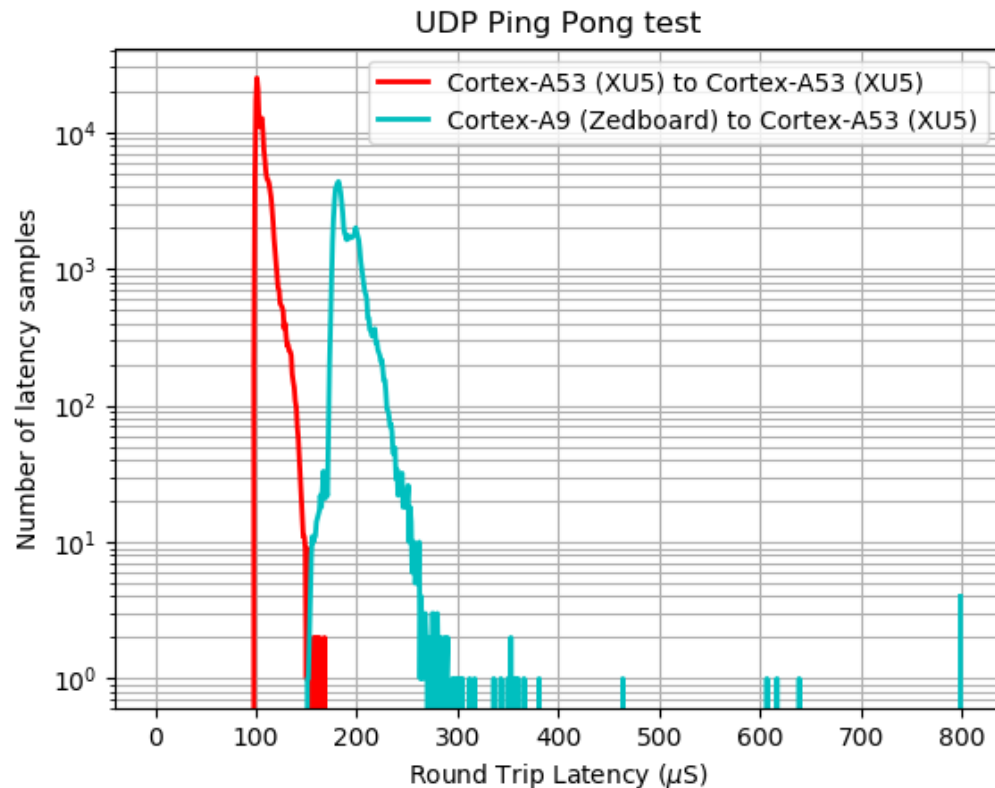
# UDP Ping Pong Test

- For Cortex-A53 to Cortex-A53 test dedicated Ethernet port is used
- Zedboard has a single Ethernet port so it is shared with SSH connections
- CPUSets not used because it adversely affected performance
- IRQ affinity changed to last CPU



# UDP Ping Pong Results

- Cortex-A53
  - Maximum: 168  $\mu\text{S}$
  - Mode: 101  $\mu\text{S}$
- Cortex-A9
  - Maximum<sub>1</sub>: >800  $\mu\text{S}$
  - Mode: 182  $\mu\text{S}$



<sub>1</sub>800  $\mu\text{S}$  was largest bin

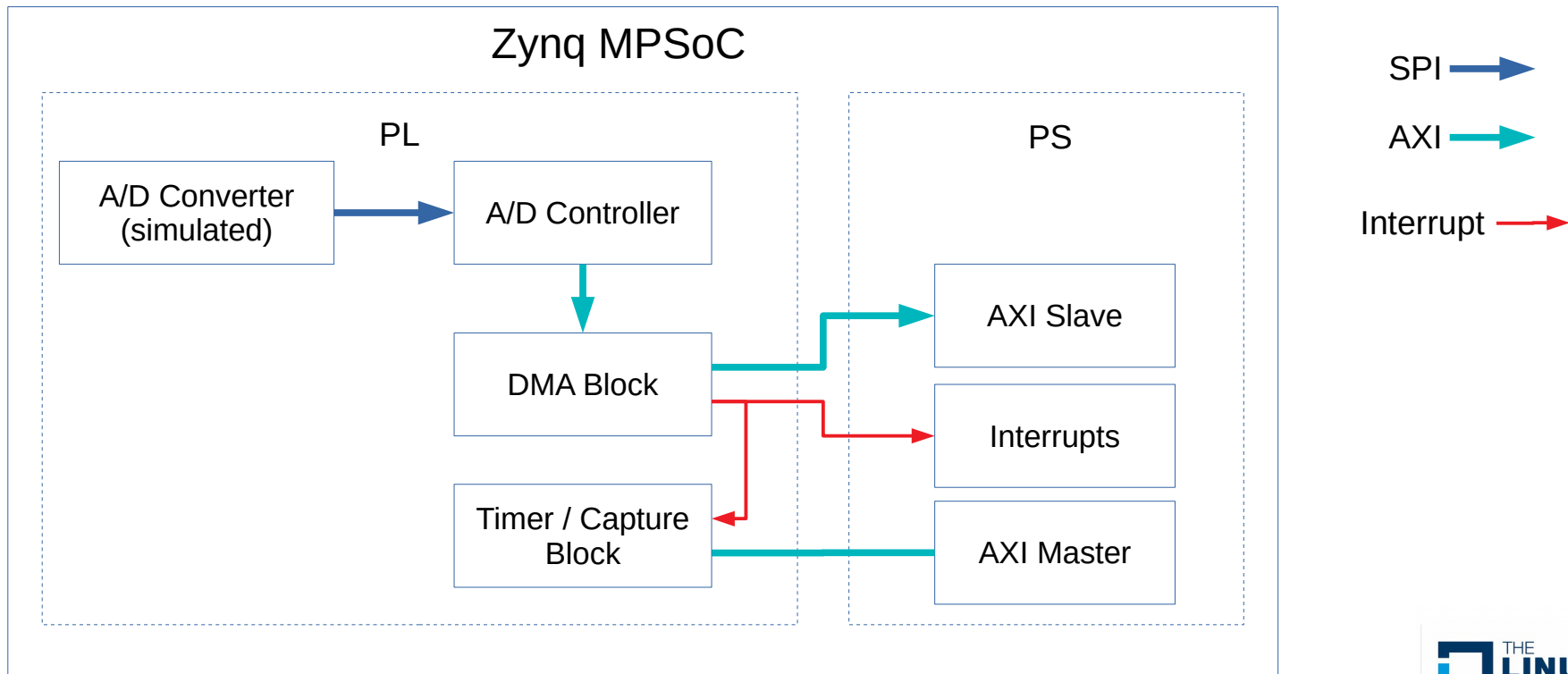
# Real World Test

- Analog to Digital Converter Driver
  - Using Industrial I/O (IIO) subsystem
  - DMA Engine based
  - Performance captured using Hardware Timer

# Industrial Input/Output (IIO)

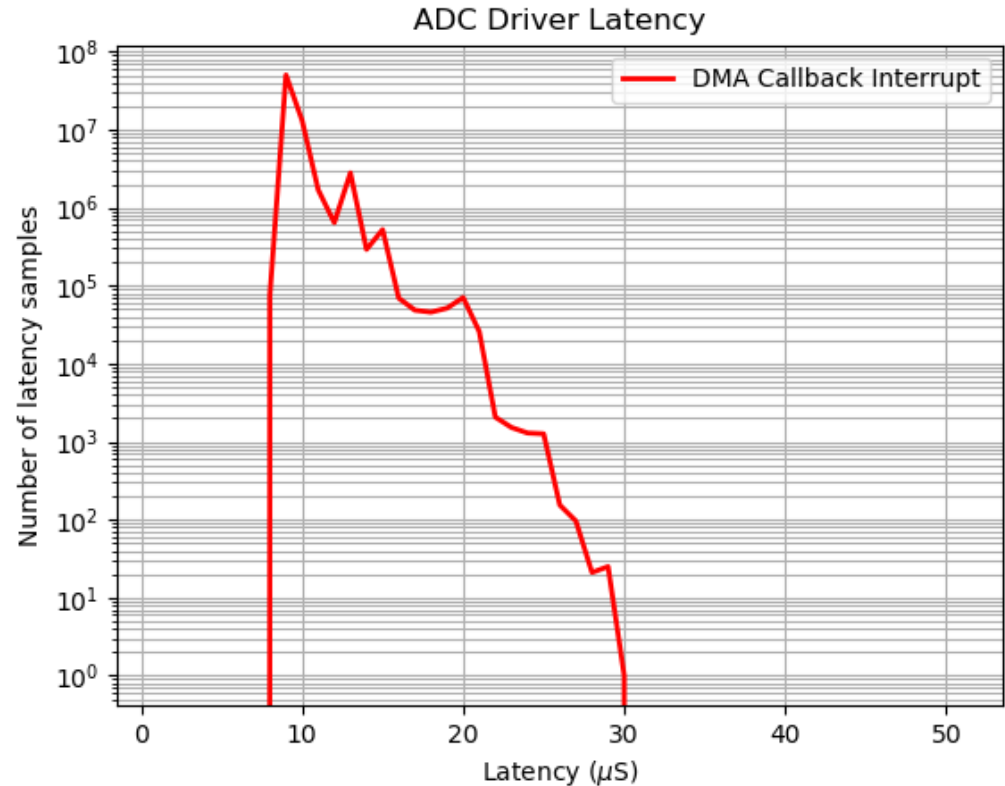
- Many Different types of devices including:
  - Analog to Digital converters
  - Digital to Analog converters
  - Accelerometers
- Can provide
  - Text formatted measurements
  - Binary ring-buffered data

# Hardware Configuration



# IIO Driver DMA Interrupt Latency

- Maximum: 30  $\mu\text{S}$
- Mode: 9  $\mu\text{S}$





# Timer Capture Function

- Hardware Timers with a capture function are common in SoCs and Microcontrollers
- Upon the trigger event the present value of the free running timer is stored to the Load Register
- In the kernel ISR (DMA Engine callback in this case) both the timer value as well as the stored Load Register from the event can be read and the latency calculated

# Conclusions

- Cortex-A53 is a very low latency core
- Using the Programmable Logic to decouple SPI bus is very effective

# Future Work

- Investigate UDP Path Latencies
  - AF\_XDP
- Investigate difference between cyclicttest and ADC driver results
- Track Preempt RT across kernel version

# Special Thanks

- Rajan Vaja from Xilinx
  - Helped us get up and running on the 4.18 kernel
- Enclustra
- My loving wife and family

