

FPGA Technology and Industry Experience

Guest Lecture at HSLU, Horw (Lucerne)

May 24 2012

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 - Company Profile
- FPGA Basics
 - FPGA Architecture
 - FPGA Design Flow
- The Case for FPGAs
 - FPGA vs. ASIC
 - FPGA vs. DSP
- Real-World FPGA Application
 - Software Defined Radio
- Example Project
 - Motion Control
- Conclusions
 - Field Update
 - Outsourcing
 - Skills
 - How to Stand Out

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- Quick Facts
 - Founded in 2004
 - Located at Technopark Zurich
 - Currently 8 employees
 - Vendor-Independent
- FPGA Design Center
 - FPGA-Related Design Services
 - Firmware (VHDL/Verilog)
 - Hardware (incl. analog and digital interfaces)
 - Embedded Software (for FPGA soft processors)

- FPGA Solution Center
 - FPGA Modules
 - Mars, Mercury and Saturn
 - IP Cores
 - TFT Display Controller
 - Universal Drive Controller
 - Etc.

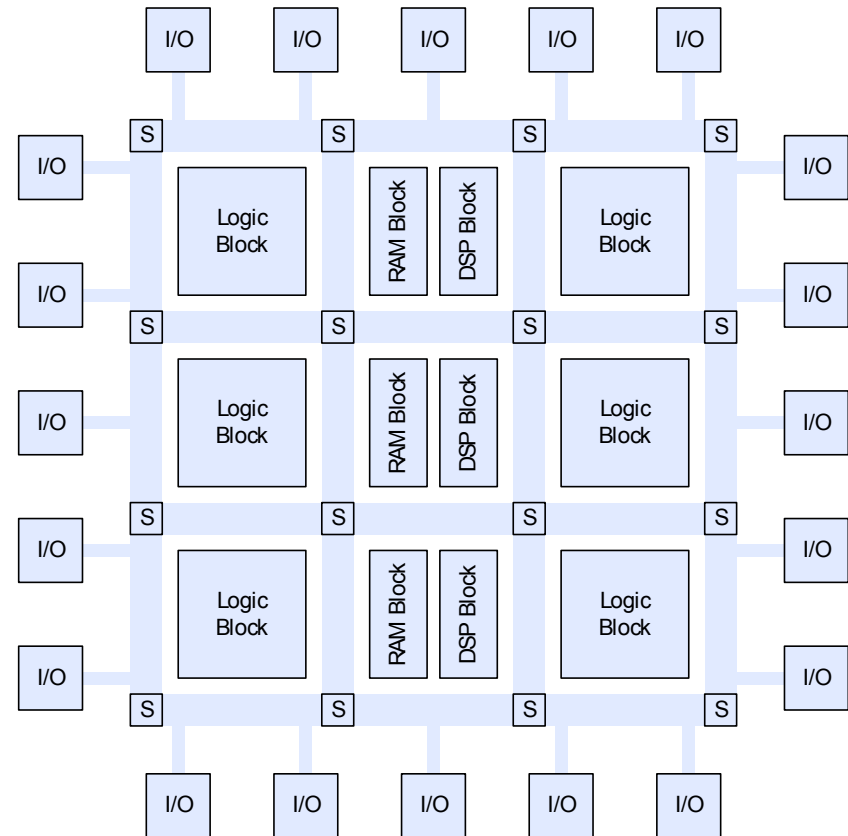


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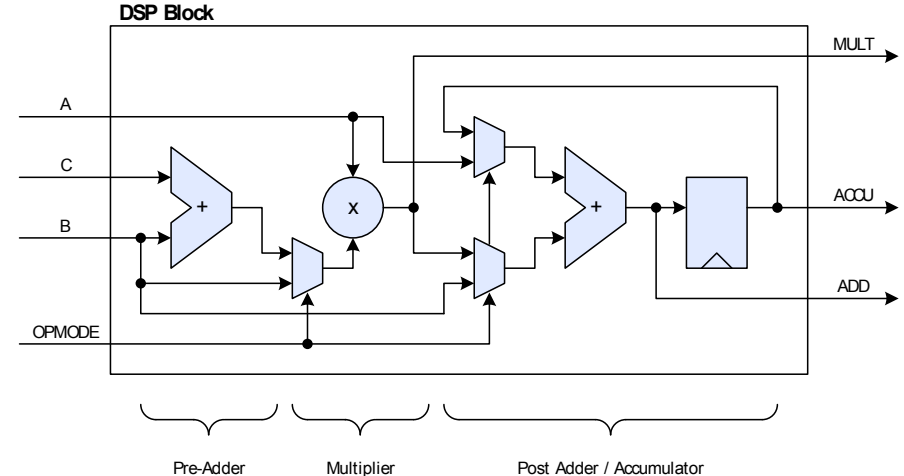
FPGA Basics – FPGA Architecture

The Big Picture

- **F**ield **P**rogrammable **G**ate **A**rray
- Regular array of configurable logic blocks
- Many Flip-Flops available
- Embedded RAM blocks
- DSP blocks
- Configurable I/O blocks
- Dedicated clock management blocks
- Configuration data stored in distributed SRAM cells



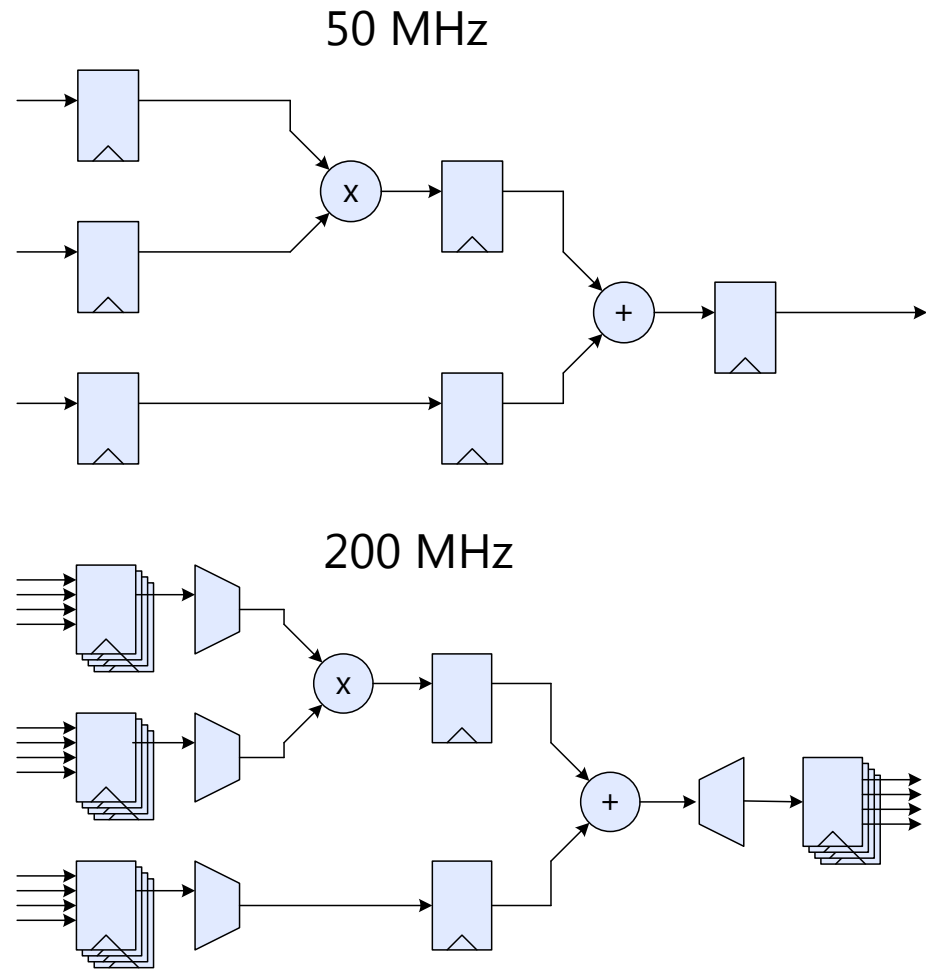
- DSP blocks are used to implement fixed-point arithmetic operations
 - Typically 18 x 18 bit multiplier
 - 48 + 48 bit adder/accumulator
 - Pre-adder for symmetric FIR filters
 - Dynamic configuration via OPMODE
 - Highly pipelined (configurable)
 - Up to 600 MHz clock frequency
 - Support for carry and adder chains
- ~4 .. 4000 per FPGA
- Up to 2400 GMAC/s per FPGA!!!



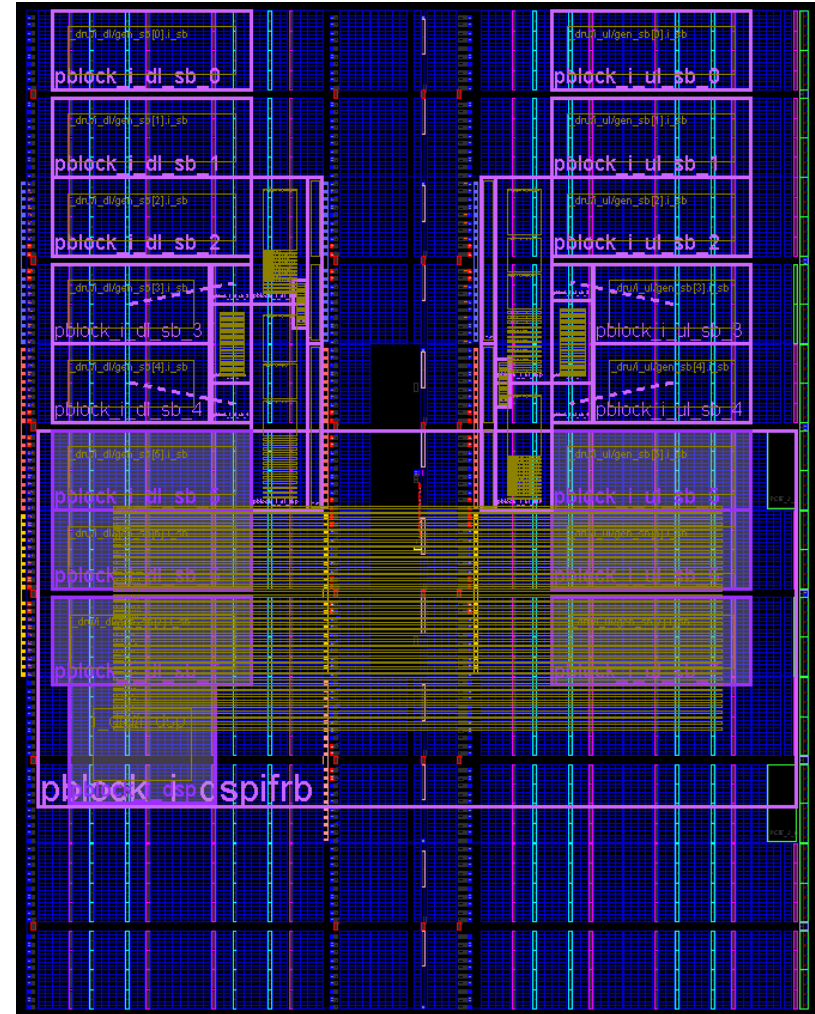
FPGA Basics – FPGA Architecture

Time Division Multiplexing (TDM)

- Register replication
 - State registers: Yes
 - Pipeline registers: No
 - BRAM/SRL can be used
- Advantages
 - Power
 - Area
 - Less hard macros
- Disadvantages
 - Longest path
 - Debugging



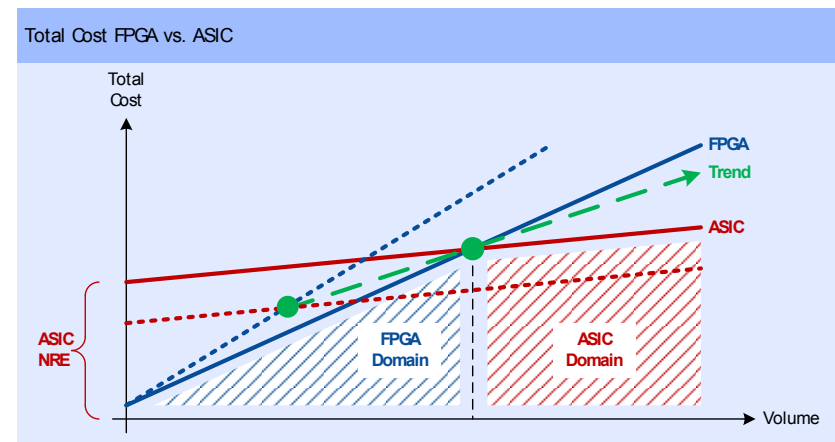
- **Floorplanning**
- Required for highest performance
- Grouping of components which belong together
- Keep floorplan in mind while designing
- Pipelining for long connections
- Placement of specific resources
- «Holes» due to hard macros
- Directions of carry chains



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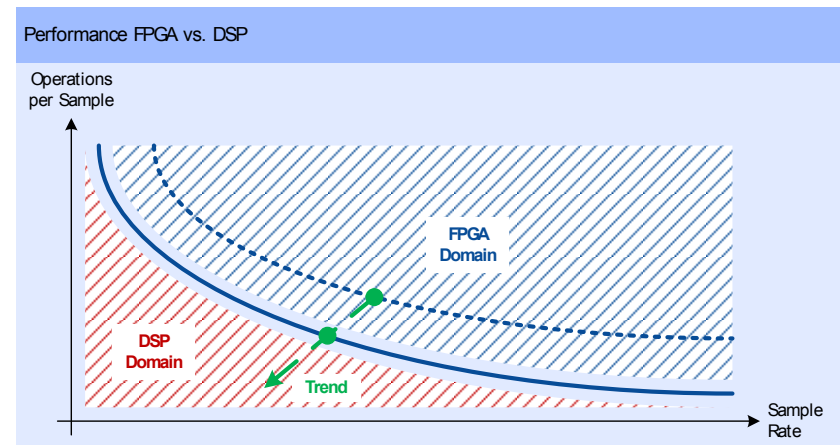
- FPGAs can't beat ASICs when it comes to
 - Low power
 - Ultra small form factor
 - Ultra high design security
 - Ultra high volume
- ASICs need volume to overcome the NRE penalty
 - NRE increase with each process shrink
 - FPGA logic gets cheaper with each process shrink
 - The break-even is moving towards higher volumes with each process shrink
- Remote update and faster time to market become more and more important
 - FPGAs gain ground in the ASIC domain
- FPGAs are often used for ASIC prototyping

| Parameter | FPGA | ASIC |
|--------------------------|------|------|
| Clock frequency | | ✓ |
| Power consumption | | ✓ |
| Form factor | | ✓ |
| Design security | | ✓ |
| Reconfiguration | ✓ | |
| Redesign risk (weighted) | ✓ | |
| NRE | ✓ | |
| Time to market | ✓ | |



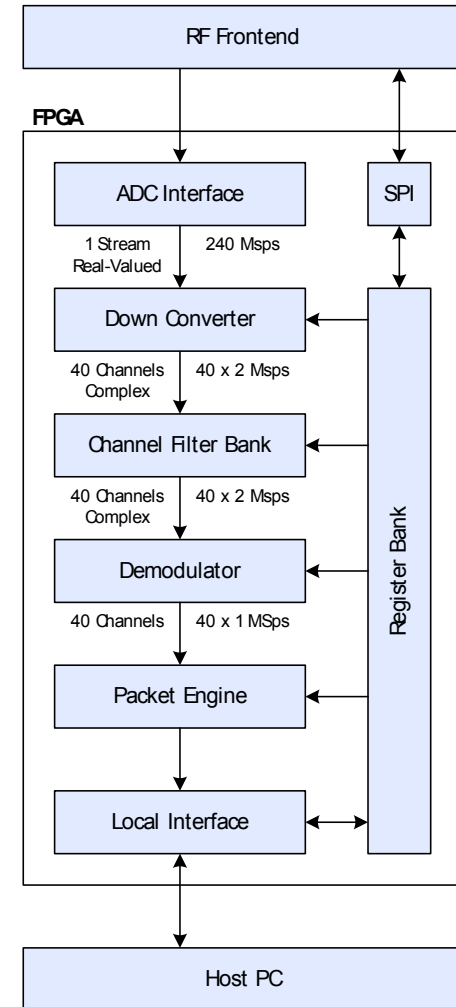
- DSPs are widely used in low-cost, low-power and low- to mid- performance systems
- DSPs suffer from their serial instruction stream when it comes to more complex systems running at high sample rates
- FPGAs can provide a performance boost of 10..1000 compared to DSPs for such applications (e.g. software defined radio).
- FPGAs even excel when compared in MAC/\$ and MAC/W.
- Hard-macro CPU cores in the FPGAs take over traditional DSP tasks (e.g. complex protocol stacks), enabling single-chip high-performance signal processing systems

| Parameter | FPGA | DSP |
|-----------------------------|------|-----|
| System performance | ✓ | |
| Multi-channel architecture | ✓ | |
| Many operations per sample | ✓ | |
| Many conditional operations | | ✓ |
| Floating point | | ✓ |
| Absolute power consumption | | ✓ |



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- Software defined radio
 - Most of the signal processing of a RF receiver/transmitter is done in „software“
- Real-world application
 - 2.4 GHz RF receiver
 - 240 Msp/s sampling rate
 - Down conversion to 40 channels at 2 Msp/s each
 - Parallel baseband-processing of all 40 channels with a time division multiplexed datapath architecture
 - Channel filters
 - Demodulators (FSK, PSK)
 - Spartan-3A DSP low-cost FPGA
 - 126 multipliers running at 240 MHz clock frequency
→ 30 giga multiplications per second
 - Ported to Spartan-6 LX
 - TDM / Floorplanning



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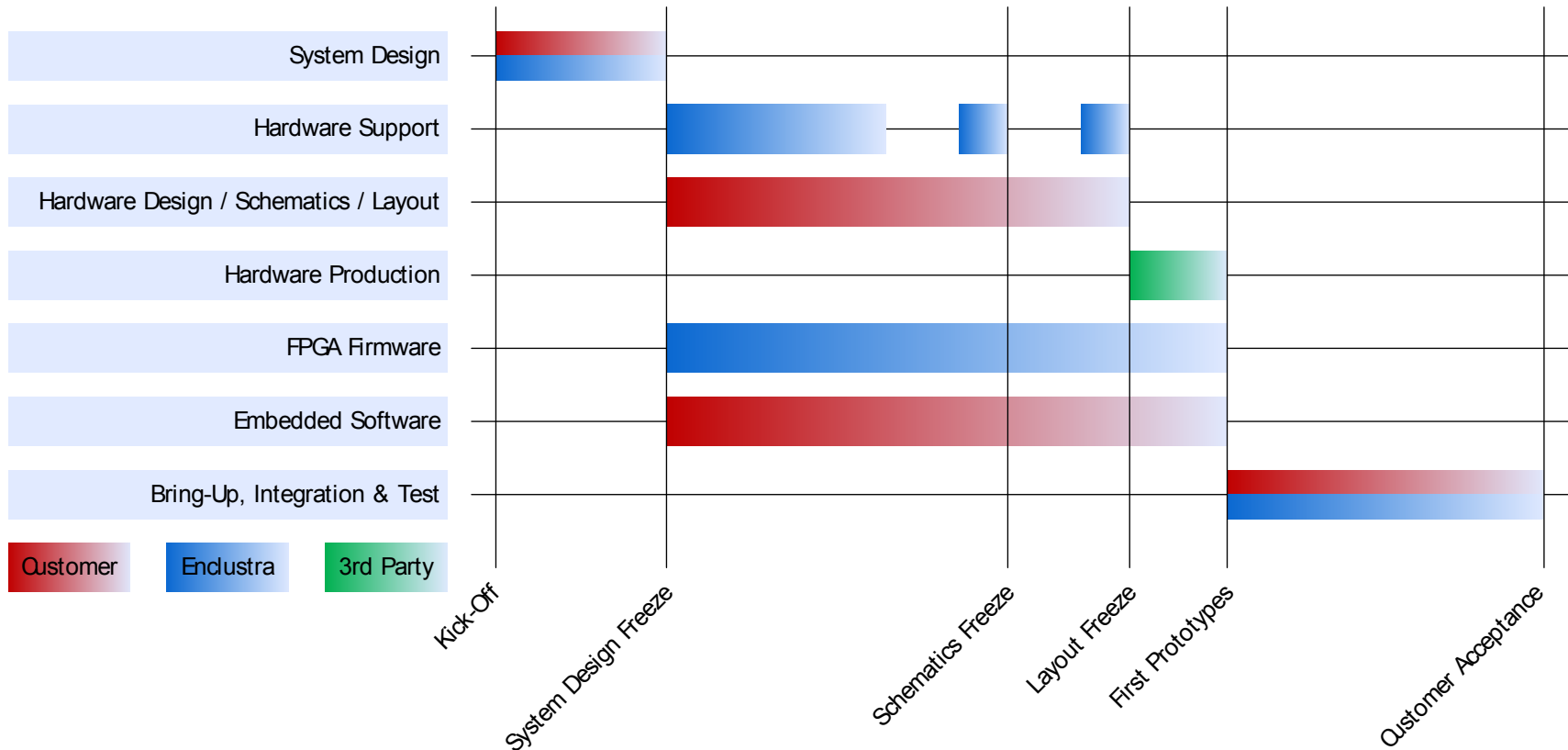
Example Project – Motion Control Specification

- Technical requirements:
 - Motion control module
 - Up to 4 DC or 2 stepper motors
 - Up to 2 BLDC motors in a later stage
 - CAN interface
 - Trajectory planner/integrator
 - 1..5 KHz position/velocity control
 - 10..100 KHz current control
 - 4 integrated FET H-bridges
 - Credit-card size
- General information:
 - Motion control platform for next-generation products
 - High-volume (> 10'000 units/year)
- Commercial requirements:
 - Manufacturing costs < X \$
 - Available no later than day Y
 - Engineering costs are secondary

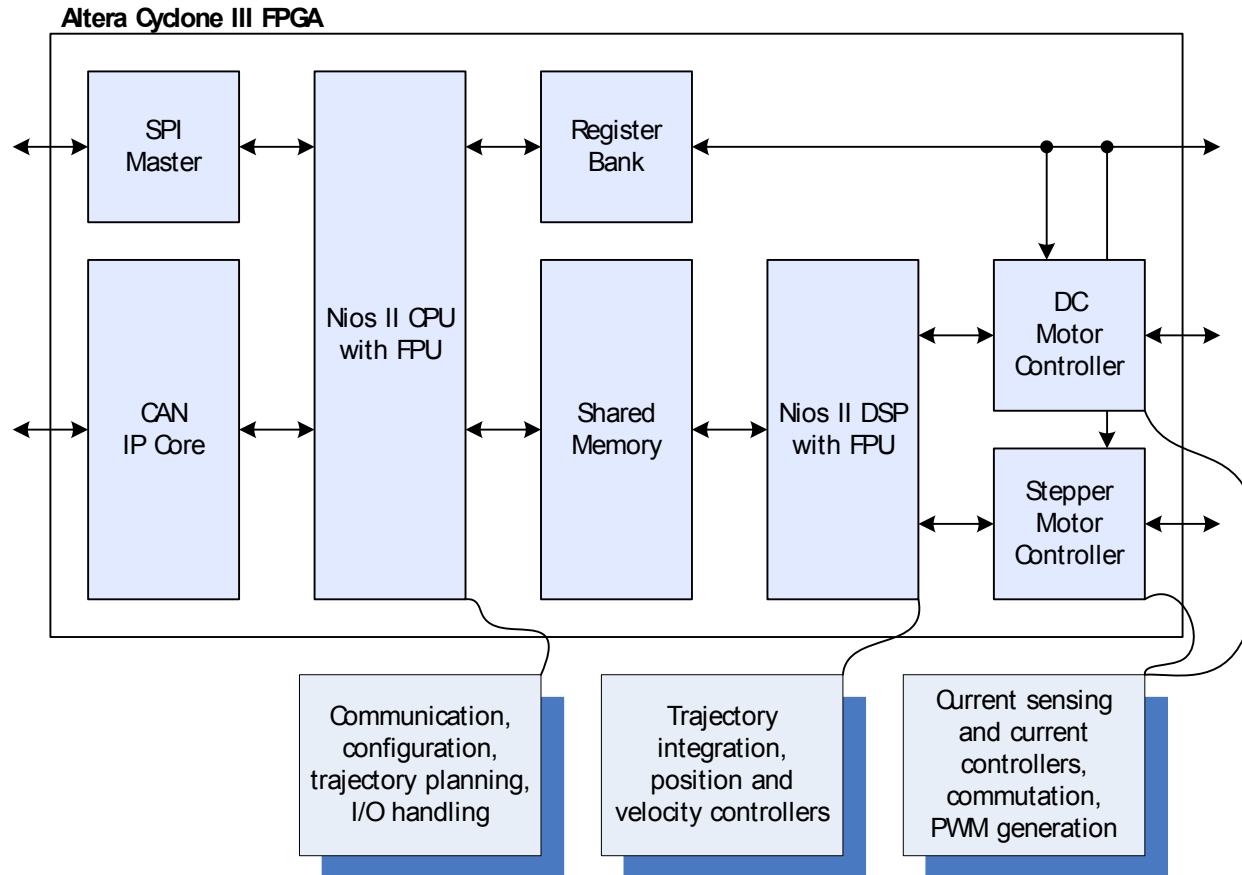
Example Project – Motion Control Project Setup

- General project setup:
 - The customer is responsible for hardware design, production and embedded software
 - Enclustra is responsible for FPGA firmware and FPGA-related system design issues
- Team setup at Enclustra:
 - 1 project manager
 - 1 FPGA firmware engineer
 - 1 hardware consultant
- Team setup at the customer:
 - 1 project manager
 - 2 embedded software engineers
 - 2 hardware engineers
 - and
 - The strategic procurement department
 - and
 - The upper management
 - and
 - Many potential users of the motion control module

Example Project – Motion Control Project Schedule (Basic Functions)

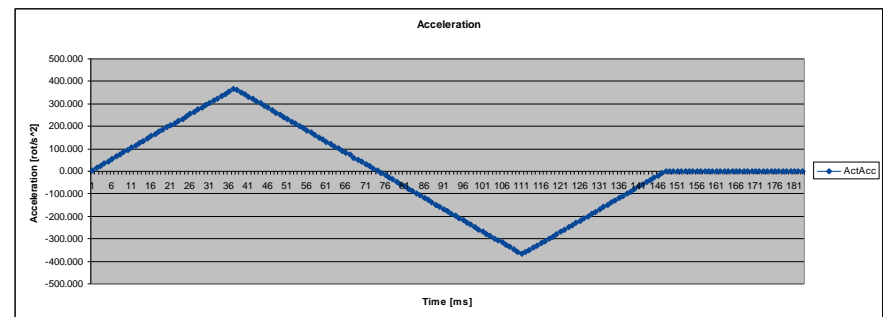
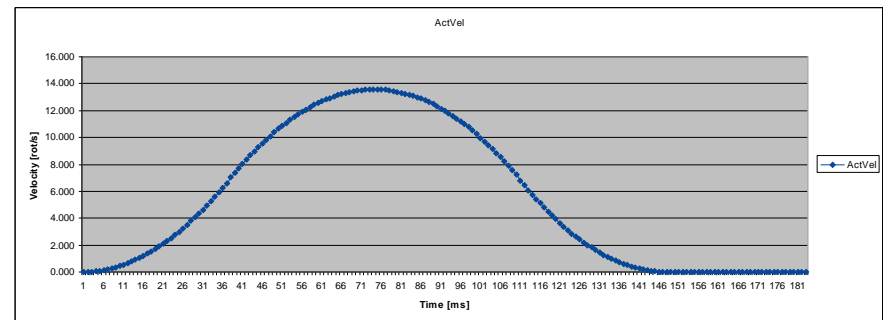
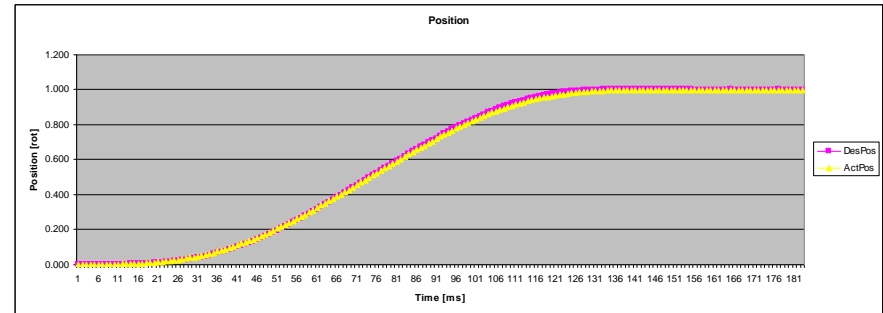
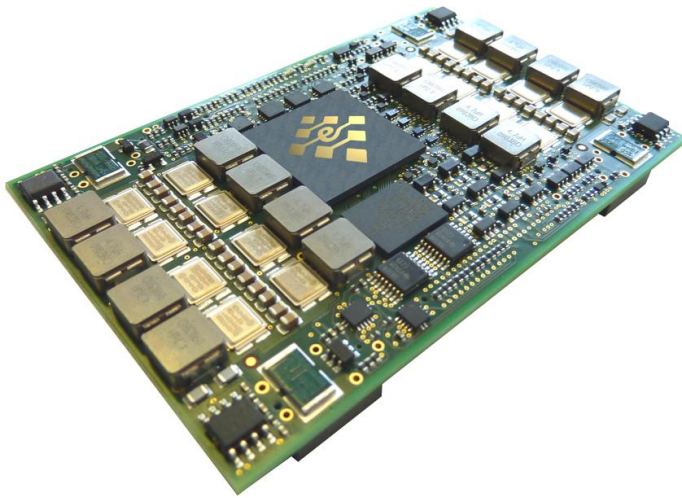


Example Project – Motion Control System Design (1)



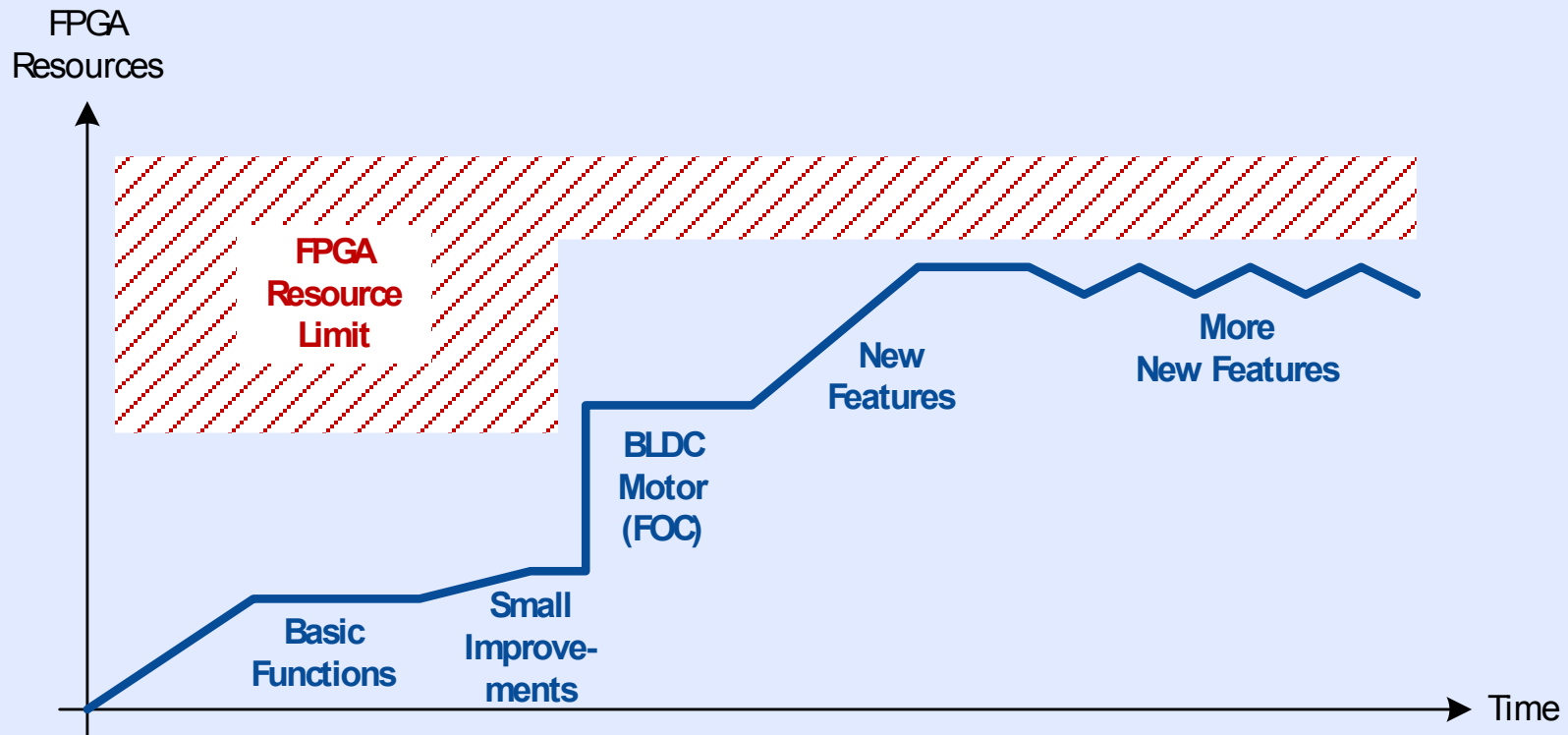
Example Project – Motion Control First Prototypes!

- Bring-Up
 - Power, clocks, FPGA configuration
 - Nios II booting and JTAG communication
- First tests on hardware
 - The first logged move!



Example Project – Motion Control FPGA Resources over Time

FPGA Resources over Time



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- **FPGAs allow fast market entry thanks to their field update capability**
- This often leads to the fallacy that FPGA development does not require thorough verification („we can fix an error after it occurs“)
 - This might be partly true for non security relevant applications running in static ambient conditions
 - FPGA development actually IS done like this a lot more than one might think
 - This often wrongs FPGA technology in the user’s minds, because there WILL be errors in this case
- The development of a reliable FPGA system does not get by without thorough verification!
 - Verification may include behavioral simulation and tests running on the hardware

- **Make or buy – the case for outsourcing FPGA development**
- Successful and efficient FPGA design requires in-depth knowledge of
 - Basic digital and analog circuit design, chip design, VLSI
 - HDL (VHDL/Verilog/etc.), FPGA architecture and tools
 - High-speed hardware design
 - Deployed algorithms, I/O standards, protocols, etc.
- Many companies have extensive knowledge in their application area, but do not have the required expertise for successfully employing FPGA technology
- Building up FPGA know-how is a lengthy and expensive process
- Collaboration between application specialists and FPGA technology experts shows great promise for successful product development

- **FPGA jobs in engineering services - what skills do we expect?**
- Technical skills
 - Basic digital and analog circuit design, chip design, VLSI (very important)
 - HDL (VHDL, Verilog, etc.)
 - Basic understanding of FPGA architecture and tools
 - Basic understanding of DSP and SoPC
- Soft skills
 - Keen perception also for complex structures
 - Good communication with customers and colleagues
 - Ability to work in a team
 - Flexibility for changing tasks quickly

- **How can an FPGA engineering company stand out from the crowd?**
- Focus on
 - FPGA technology (don't be a „general merchandise store“)
 - Key application domains (e.g. DSP, SoPC, etc.)
- Provide solutions, not only engineering resources
 - FPGA modules as HW platform
 - IP cores for complex building blocks
 - Custom design for custom functionality
 - System integration
- Not only make the customer happy, but also make him successful
 - What the customer initially wants is most often not what he really needs



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Slides in PDF format:

<http://www.enclustra.com/de/company/publications/>