Generic High-Performance DSP Library for FPGAs

Embedded Computing Conference 2021

Dr. Harry Commin | Enclustra GmbH | 01 June 2021

Agenda

- *Enclustra*
- *Introduction to Universal DSP Library*
- *On-Screen Demonstration*
  - *Build a simple DSP system in Vivado*
  - *Run on hardware*
  - *Bit-true software modelling*

Focused on FPGA Technology – Everything FPGA!

Founded in 2004, >50 employees, based in Zurich.

Branch offices in Germany, USA and China.

XILINX. ALLIANCE PROGRAM CERTIFIED MEMBER — BASE

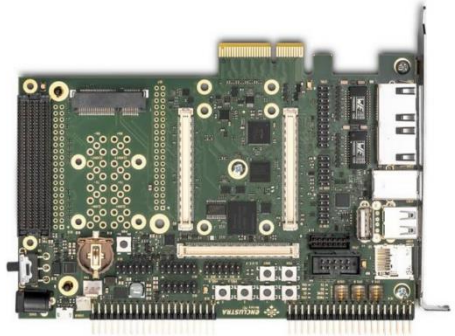
intel FPGA Design Solutions Network Gold

LEADER Lattice Exclusive Alliance of Design Engineering Resources

Microsemi

MathWorks Partner

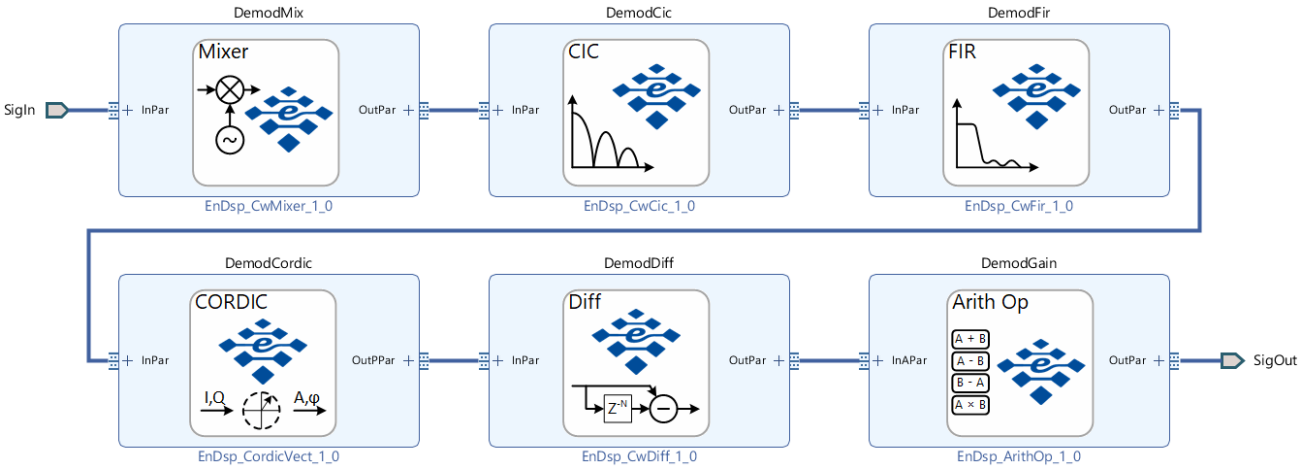
- *FPGA Design Center*
  - *Hardware (High-Speed, Analog, RF)*
  - *HDL firmware (VHDL, Verilog)*
  - *Embedded software (for FPGA processors)*
- *FPGA Solution Center*
  - *FPGA & SoC Modules*
  - *IP Cores*



- *The problem:*
  - *Many DSP designs use the same functional blocks*
    - *DSP: Filters, mixers, CORDIC, function approximations, …*
    - *Glue Logic: (De)multiplexers, buffers, TDM-parallel converters, …*
  - *Minor differences in requirements lead to major development effort*
    - *Single-channel, parallel channels, TDM*
    - *Continuous wave (CW) or pulse processing*
    - *Real or complex signals*
    - *Incompatible interfaces*

⇒ Too much time is spent implementing the most common DSP functionality.

- *The opportunity:*
  - *FPGAs are getting better (cost, timing, power)*
    - *Many customers prefer to sacrifice a few FPGA resources / timing performance / power consumption to reduce development cost and risk*
  - *Graphical design tools (e.g. Vivado IP Integrator) are improving*



- *Existing Solutions?*
  - *Xilinx IP*
    - *Very limited DSP functionality available*
    - *Inconsistency between different DSP blocks*
  - *MATLAB/Simulink HDL Coder*
    - *Expensive seat-based licenses*
    - *Delay in support for FPGA synthesis tool (Vivado) support*
  - *NI LabVIEW*
    - *Requires NI hardware*
    - *Delay in support for FPGA synthesis tool (Vivado) support*

Universal DSP Library (EN-DSP)

- *Enclustra's Universal DSP Library (EN-DSP)*
  - *Simple common interface convention (based on AXI4-Stream)*
    - *Supports parallel and TDM channels*
    - *Supports CW and pulse processing*
    - *Supports real and complex signals*
  - *Integrates with Vivado IP Integrator*
    - *Awaiting graphical tools from other FPGA vendors*
  - *Uses free open-source VHDL / Python / TCL libraries from the Paul Scherrer Institute (PSI)*
    - *Bit-true software models for every DSP block*
    - *Vivado IPI packaging*

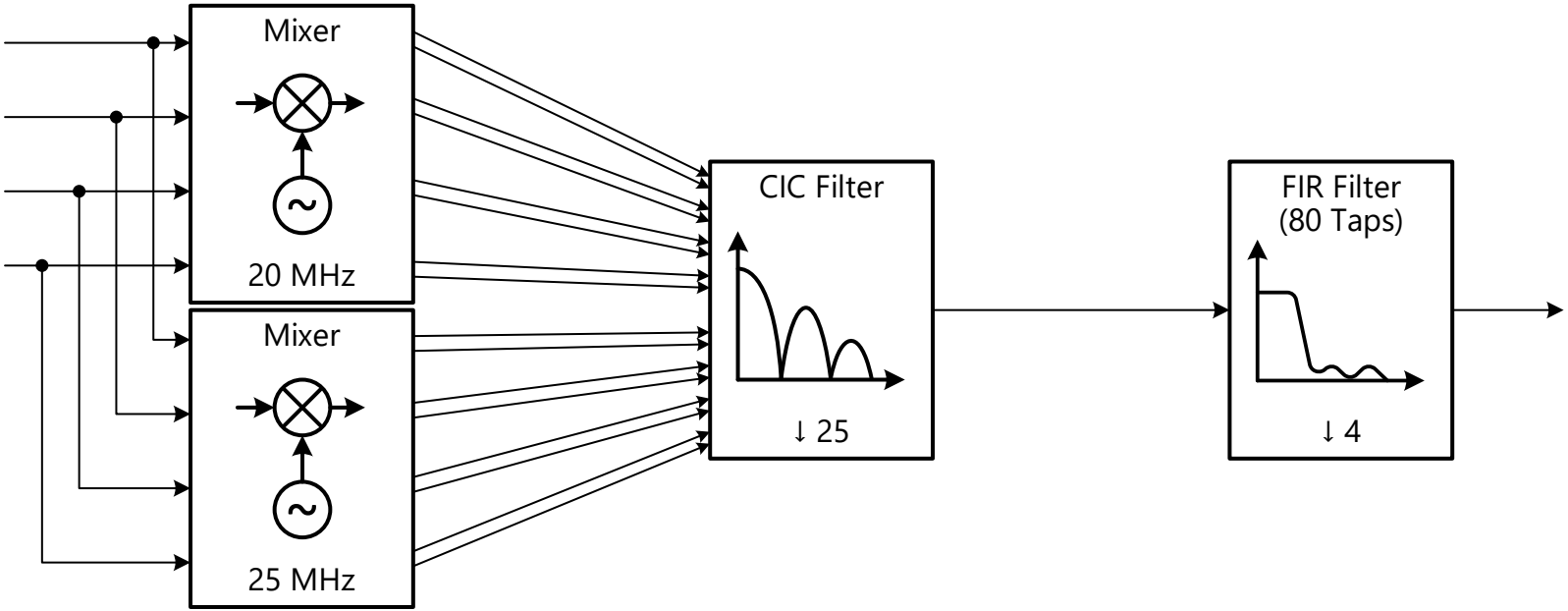
Demonstration

4 × 100 MSps
Parallel
16-bit (real)

16 × 100 MSps
Parallel
18-bit (complex)

16 × 4 MSps
TDM
18-bit (complex)

16 × 1 MSps
TDM
18-bit (complex)



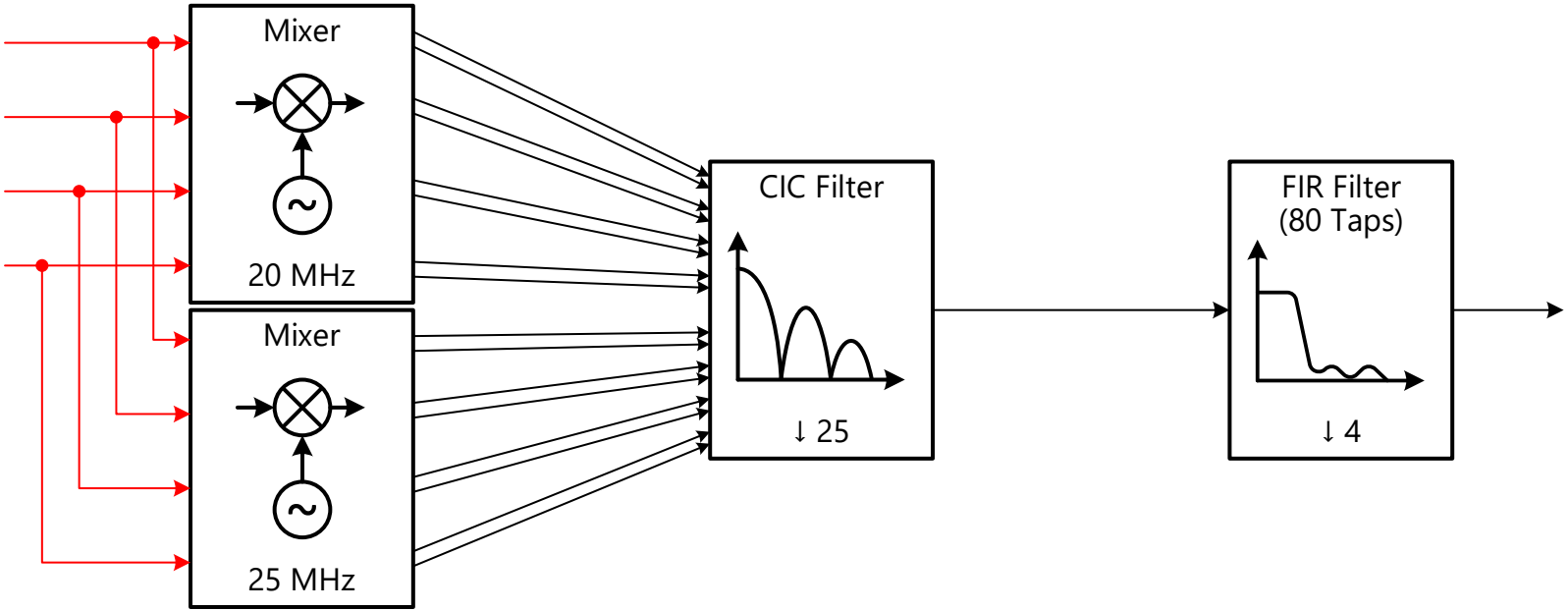
Demonstration

4 × 100 MSps
Parallel
16-bit (real)

16 × 100 MSps
Parallel
18-bit (complex)

16 × 4 MSps
TDM
18-bit (complex)

16 × 1 MSps
TDM
18-bit (complex)



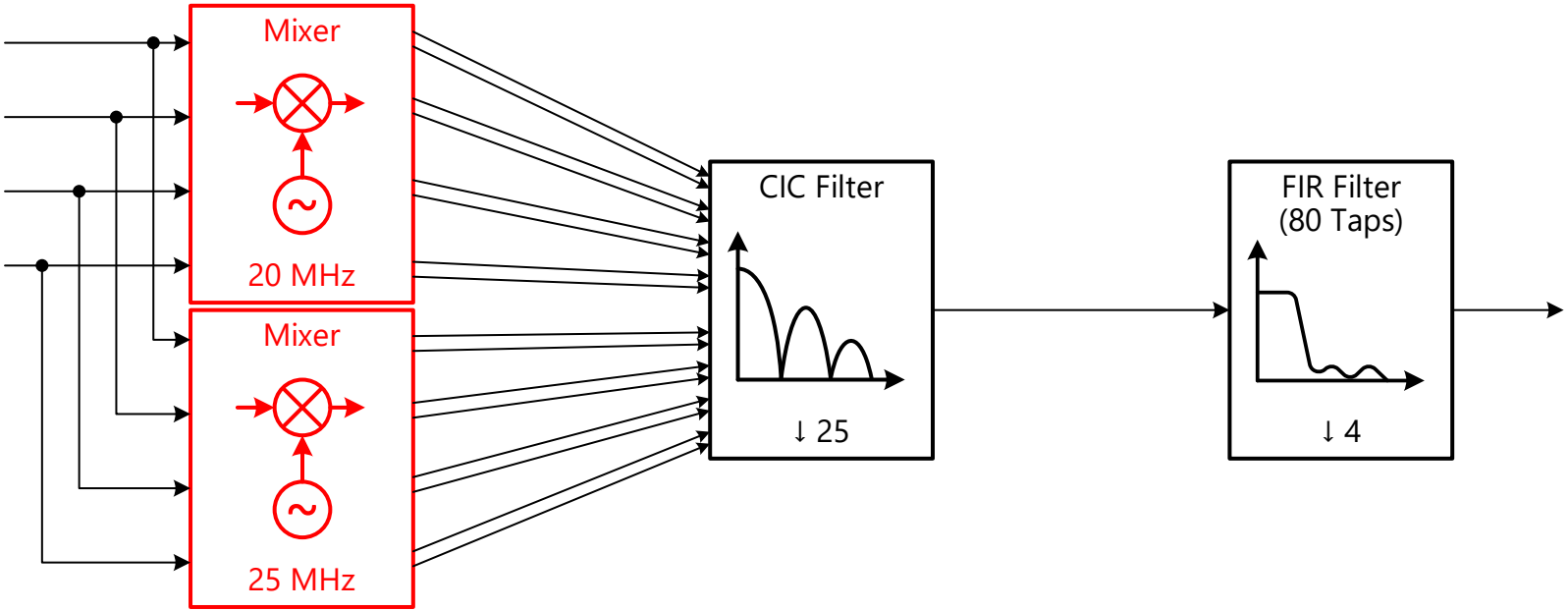
Demonstration

4 × 100 MSps
Parallel
16-bit (real)

16 × 100 MSps
Parallel
18-bit (complex)

16 × 4 MSps
TDM
18-bit (complex)

16 × 1 MSps
TDM
18-bit (complex)



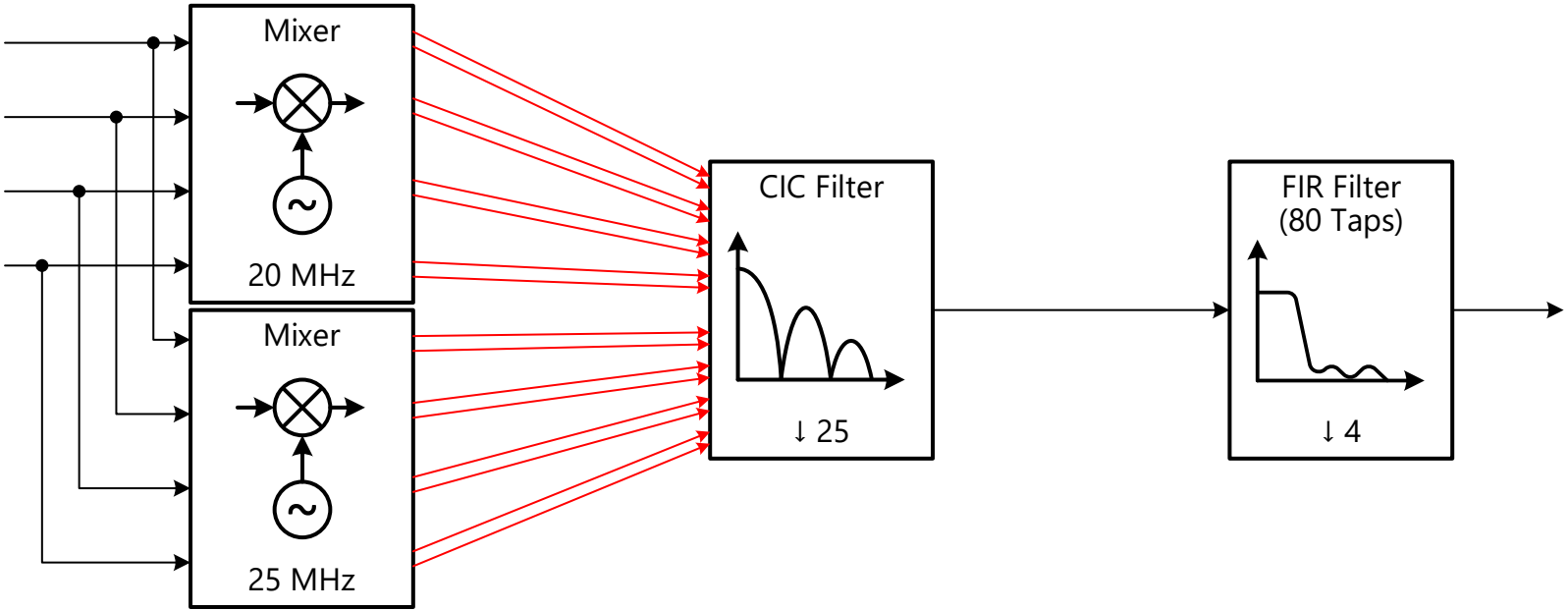
Demonstration

4 × 100 MSps
Parallel
16-bit (real)

16 × 100 MSps
Parallel
18-bit (complex)

16 × 4 MSps
TDM
18-bit (complex)

16 × 1 MSps
TDM
18-bit (complex)



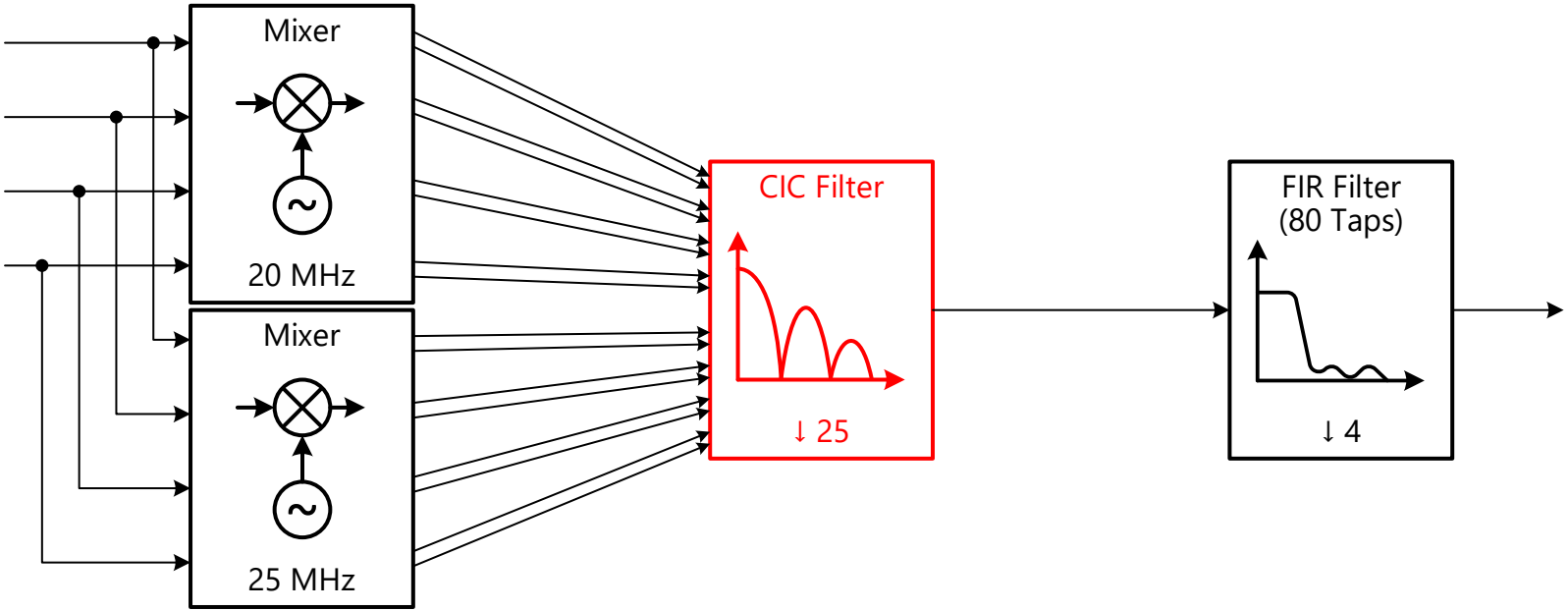
Demonstration

4 × 100 MSps
Parallel
16-bit (real)

16 × 100 MSps
Parallel
18-bit (complex)

16 × 4 MSps
TDM
18-bit (complex)

16 × 1 MSps
TDM
18-bit (complex)



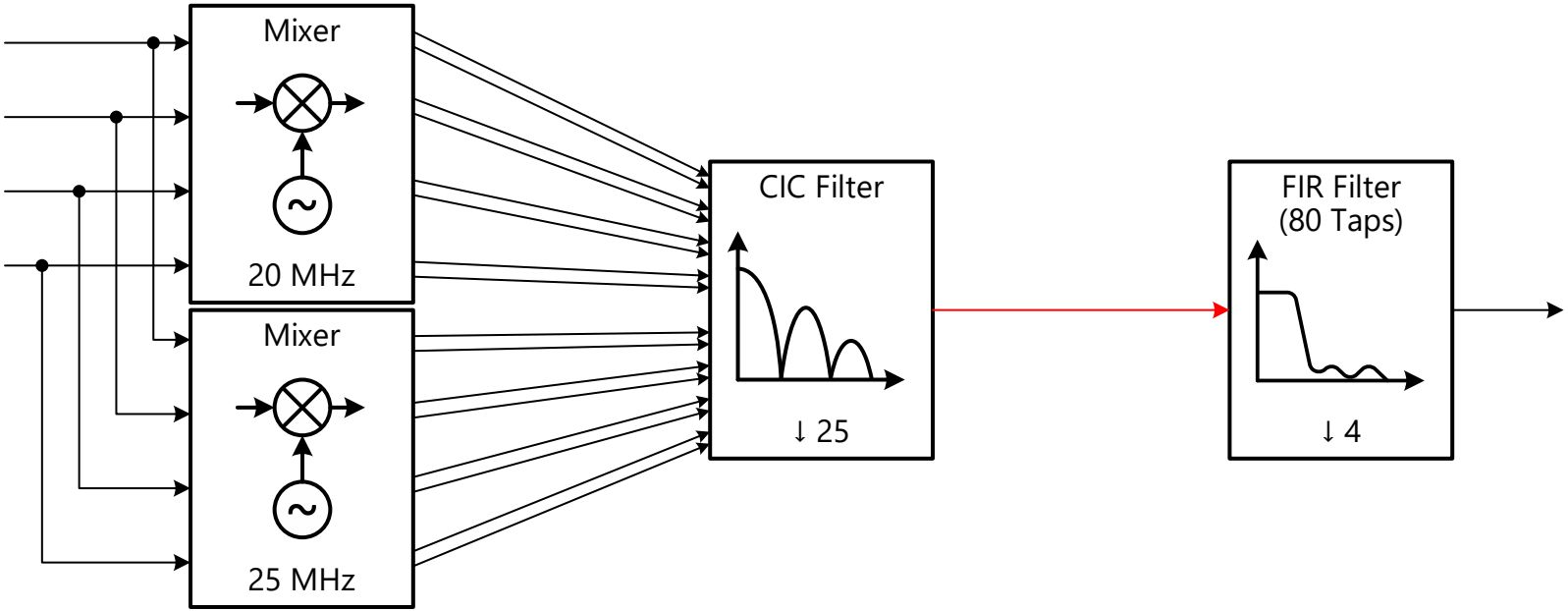
Demonstration

4 × 100 MSps
Parallel
16-bit (real)

16 × 100 MSps
Parallel
18-bit (complex)

16 × 4 MSps
TDM
18-bit (complex)

16 × 1 MSps
TDM
18-bit (complex)



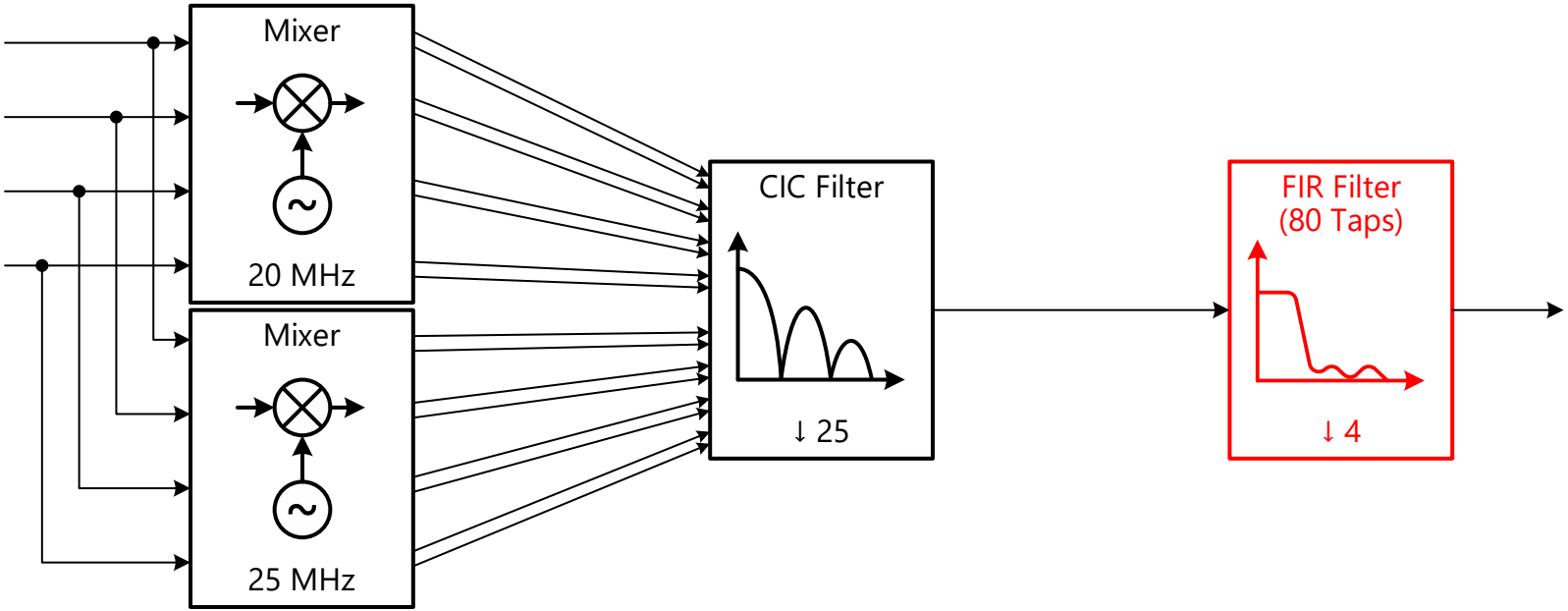
Demonstration

4 × 100 MSps
Parallel
16-bit (real)

16 × 100 MSps
Parallel
18-bit (complex)

16 × 4 MSps
TDM
18-bit (complex)

16 × 1 MSps
TDM
18-bit (complex)



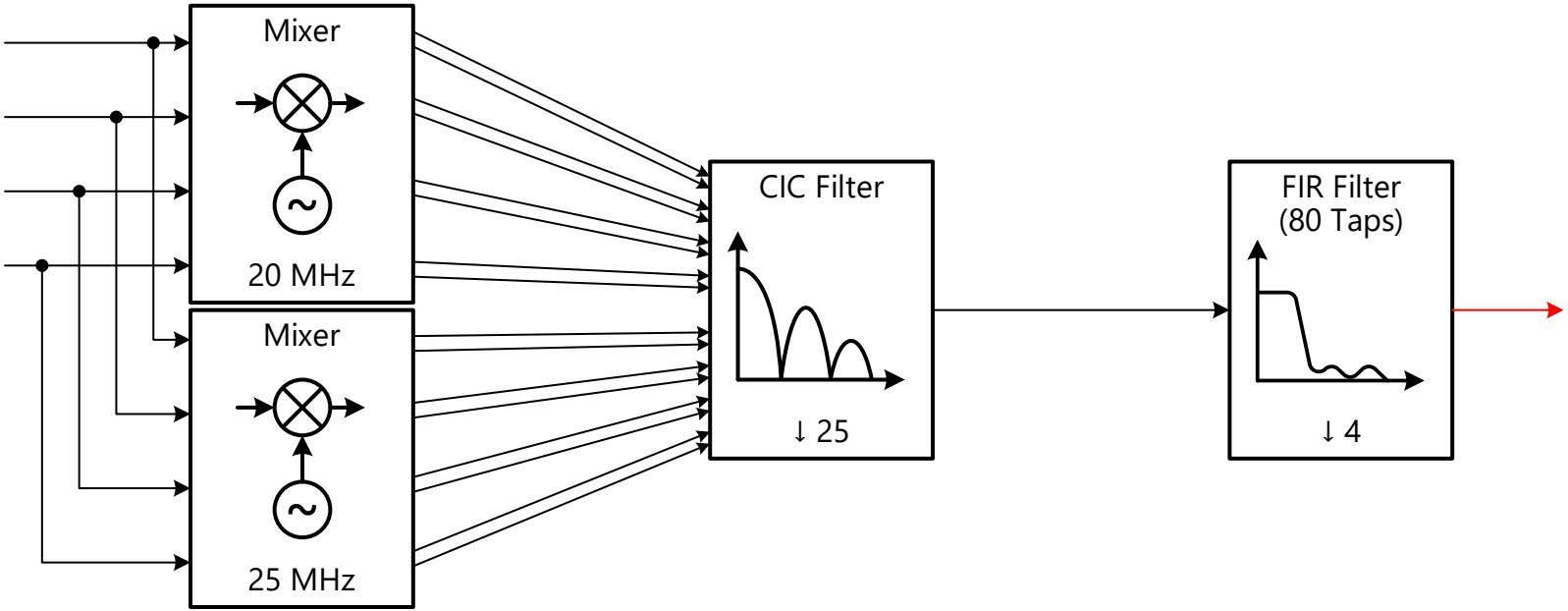
Demonstration

4 × 100 MSps
Parallel
16-bit (real)

16 × 100 MSps
Parallel
18-bit (complex)

16 × 4 MSps
TDM
18-bit (complex)

16 × 1 MSps
TDM
18-bit (complex)



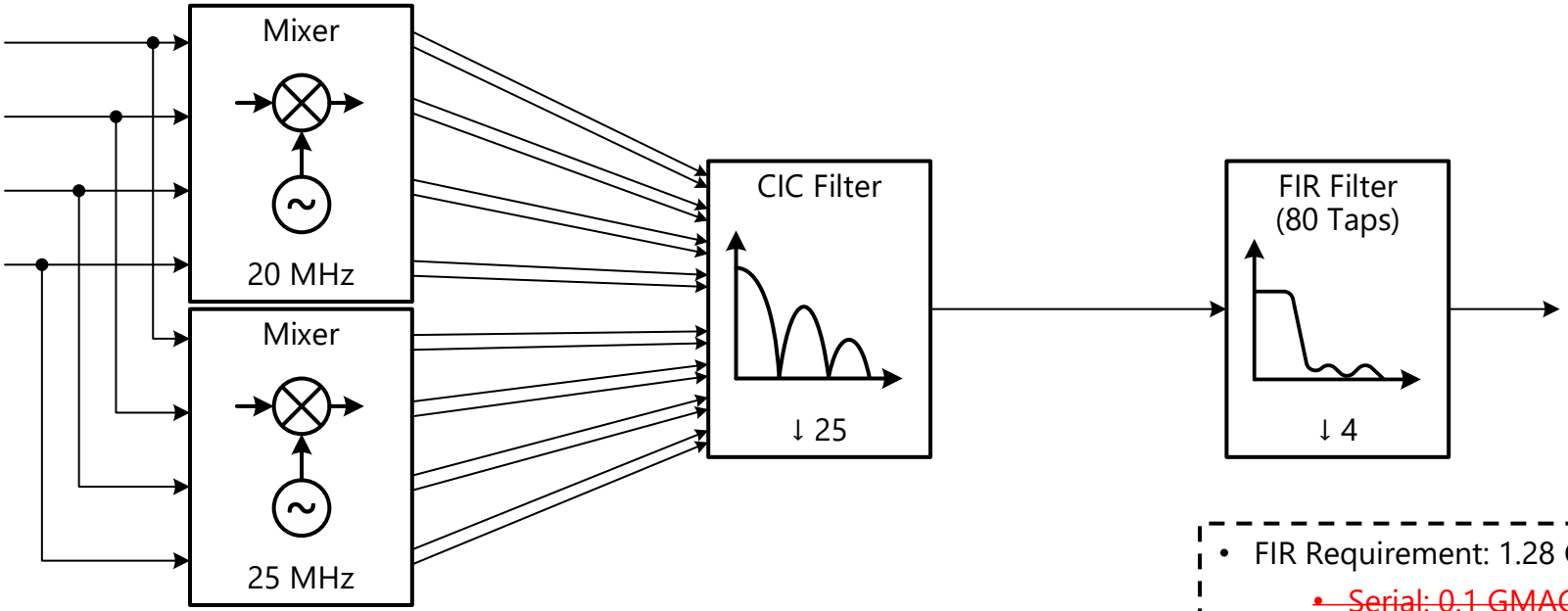
Demonstration

4 × 100 MSps
Parallel
16-bit (real)

16 × 100 MSps
Parallel
18-bit (complex)

16 × 4 MSps
TDM
18-bit (complex)

16 × 1 MSps
TDM
18-bit (complex)



- FIR Requirement: 1.28 GMACs
  - ~~Serial: 0.1 GMACs~~
  - ~~Parallel taps: 8.0 GMACs~~
  - Parallel channels: 1.6 GMACs

Summary

- *Built a simple DSP system in Vivado without writing any HDL*
- *Ran in hardware*
- *Verified the hardware output against a bit-true software model*

Everything FPGA.