



Overview

The Enclustra TFT Display Controller IP Core enables the easy addition of a TFT display to existing or future FPGA designs. It allows the system designer to focus on the main application instead of dealing with ancillary TFT display control issues. In addition, there is no need for an external display controller device that would consume precious PCB space and unnecessarily extend the project's BOM.

With its modular design and strong scalability, the TFT Display Controller IP Core perfectly fits the system requirements without wasting any FPGA resources. These unique features will also simplify the reuse of the TFT Display Controller IP Core in future projects.

Selecting Enclustra's TFT Display Controller IP Core for the TFT display control needs of present or future projects will significantly reduce time to market as well as the overall system cost.



Highlights

- Support for parallel, LVDS and DVI displays without external display controller device
- Support for unlimited video pages
- Built-in PWM generator for display brightness control
- Optional 2D accelerator unit (draw/copy rectangles, supports transparent color)

Features

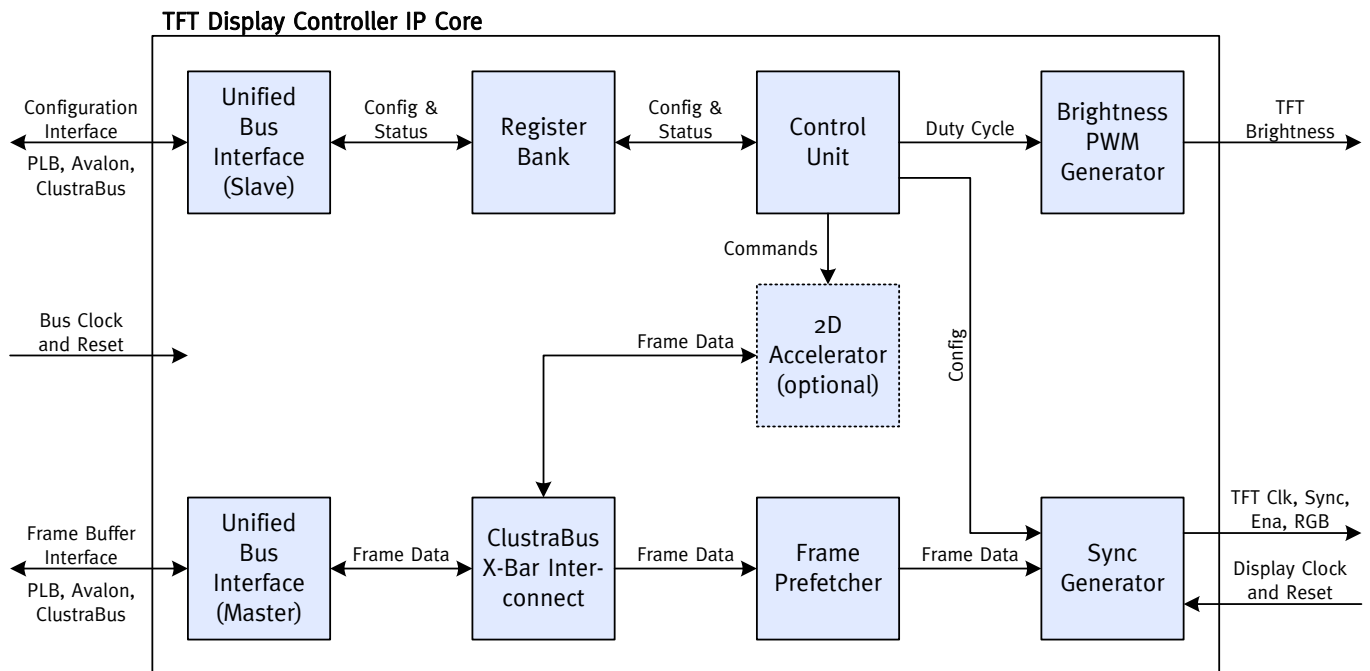
- Supported color modes:
 - 16 bit true color (5/6/5)
 - 8 bit palette with 16 bit look-up table
- Supported display resolutions:
 - Up to 1280x1024 on low-cost FPGAs*
 - Up to 1920x1080 on high-performance FPGAs*
- Unified bus interface (slave) for register bank access (Avalon, PLB, ClustraBus, 16 or 32 bit)
- Unified bus interface (master) for frame buffer memory access (Avalon, PLB, ClustraBus, 16, 32 or 64 bit)

Benefits

- No need for an external display controller device which results in a smaller PCB and a reduced BOM
- Low resource usage and good scaling due to modular design
- Easy integration thanks to the unified bus interface and the clearly laid out register bank



Core Architecture



Core Architecture Facts

- Display clock and bus clock may be different clock signals. Synchronization is taken care of inside the TFT display controller IP core
- The 2D accelerator block is optional, it is only implemented if required
- The register bank is accessible via a PLB, Avalon or ClustraBus bus interface
- The frame buffer memory can be attached to the TFT display controller IP core via a PLB, Avalon or ClustraBus interface

Related Products

- Enclustra Mars MX1, MX2, AX3* FPGA Module
- Enclustra Mars ZX2* Embedded Processing Module
- Enclustra Mars Starter Base Board
- Enclustra Mercury CA1 FPGA Module
- Enclustra Mercury Starter Base Board

Target Applications

- Industrial Automation
- Embedded Computing
- Consumer Electronics
- Display

Deliverables

- FPGA-specific netlist & VHDL component declaration
- Precompiled simulation library (ModelSim PE)
- VHDL test bench with bus functional model
- User manual

* Future product, not yet available.